

FEATURES

- VCC Current (Commercial/Industrial)
 - Operating: 70mA/85mA
 - CMOS Standby: 150µA/150µA
- Access Times
 - 55/70/100 ns (Commercial or Industrial)
- Single 5V±10% Power Supply
- Easy Memory Expansion Using \overline{CE}_1 , CE_2 , and \overline{OE}
- Common Data I/O
- Three-State Outputs
- Fully TTL Compatible Inputs and Outputs
- Advanced CMOS Technology
- Automatic Power Down
- Packages
 - 32-Pin 600 mil Plastic and Ceramic DIP
 - 32-Pin 445 mil SOP
 - 32-Pin TSOP
 - 32-Pin LCC (400x820 mil) [Two-Sided]



DESCRIPTION

The P4C1024L is a 1,048,576-bit low power CMOS static RAM organized as 128Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

Access times of 55 ns, 70 ns, and 100 ns are available. CMOS is utilized to reduce power consumption to a low level.

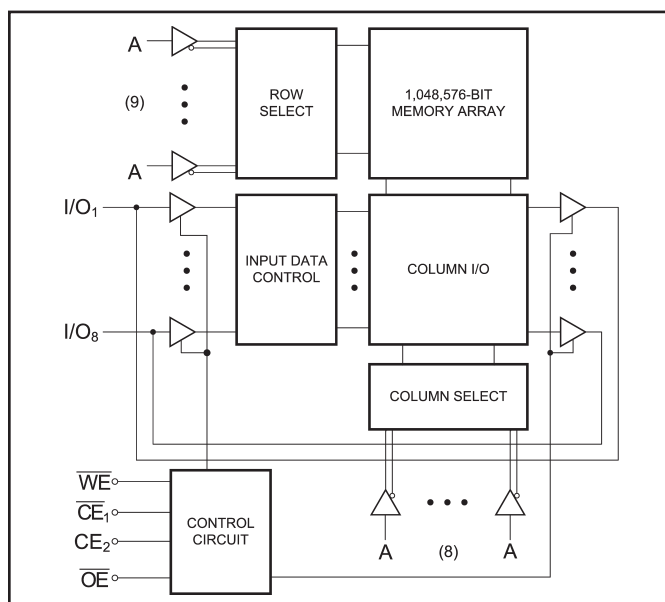
The P4C1024L device provides asynchronous operation with matching access and cycle times. Memory locations

are specified on address pins A_0 to A_{16} . Reading is accomplished by device selection (\overline{CE}_1 low and CE_2 high) and output enabling (\overline{OE}) while write enable (\overline{WE}) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either CE_1 or \overline{OE} is HIGH or \overline{WE} or \overline{CE}_2 is LOW.

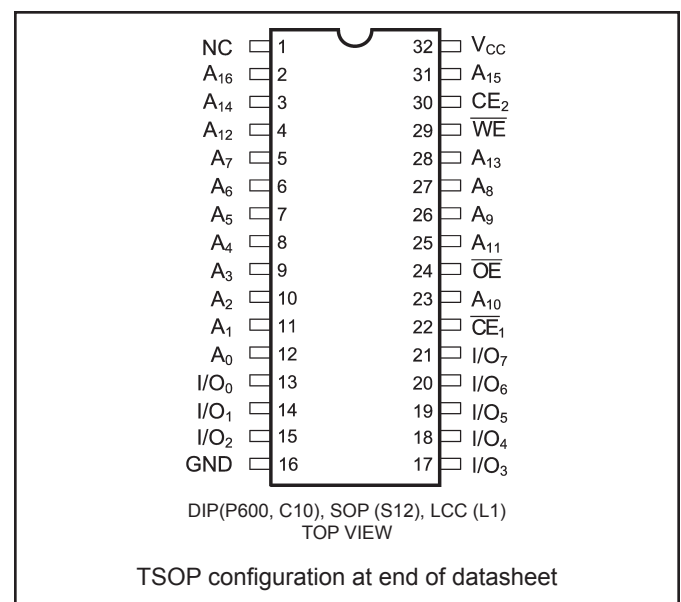
The P4C1024L is packaged in a 32-pin TSOP, 445 mil SOP, 600 mil PDIP, or 32-pin LCC package.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS





MAXIMUM RATINGS⁽¹⁾

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to $V_{CC} + 0.5$	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	Output Current into Low Outputs		mA
I_{LAT}	Latch-up Current		mA

RECOMMENDED OPERATING CONDITIONS

Grade ⁽²⁾	Ambient Temp	GND	V_{CC}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES⁽⁴⁾

($V_{CC} = 5.0V$, $T_A = 25^\circ C$, $f = 1.0MHz$)

Sym	Parameter	Conditions	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	7	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)⁽²⁾

Sym	Parameter	Test Conditions	Min	Max	Unit	
V_{OH}	Output High Voltage ($I/O_0 - I/O_7$)	$I_{OH} = -1mA$, $V_{CC} = 4.5V$	2.4		V	
V_{OL}	Output Low Voltage ($I/O_0 - I/O_7$)	$I_{OL} = 2.1mA$		0.4	V	
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage		-0.5	0.8	V	
I_{LI}	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	MIL	-10	+10	μA
			IND	-5	+5	
			COM	-2	+2	
I_{LO}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, $CE_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$	MIL	-10	+10	μA
			IND	-5	+5	
			COM	-2	+2	
I_{SB}	V_{CC} Current TTL Standby Current (TTL Input Levels)	$V_{CC} = 5.5V$, $I_{OUT} = 0mA$ $CE_1 = V_{IH}$ or $CE_2 = V_{IL}$		3	mA	
I_{SB1}	V_{CC} Current CMOS Standby Current (CMOS Input Levels)	$V_{CC} = 5.5V$, $I_{OUT} = 0mA$ $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$		50	μA	



POWER DISSIPATION CHARACTERISTICS

Sym	Parameter	Temperature Range	*			**			Unit
			-55	-70	-100	-55	-70	-100	
I _{CC}	Dynamic Operating Current	Commercial	70	70	70	15	15	15	mA
		Industrial/Military	85	85	85	25	25	25	mA

* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}_2 \geq V_{IH}$ (min), \overline{CE}_1 and $\overline{WE} \leq V_{IL}$ (max), \overline{OE} is high. Switching inputs are 0V and 3V.

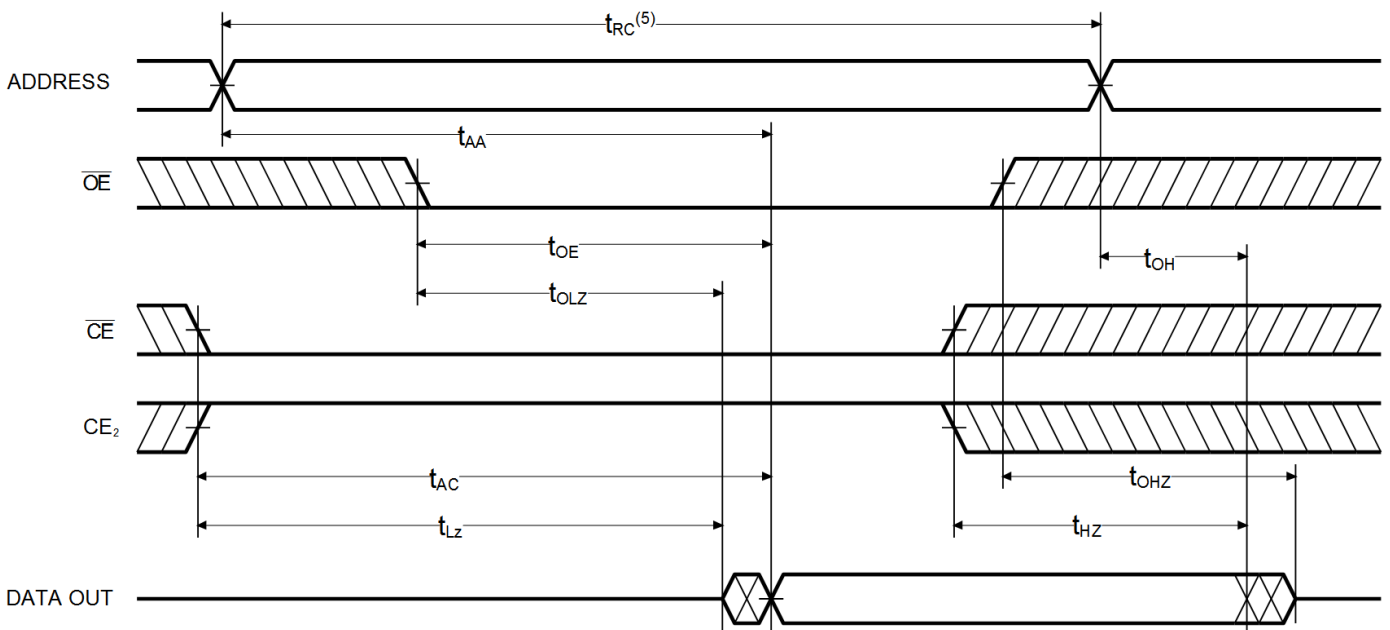
** As above but @ f=1 MHz and $V_{IL} / V_{IH} = 0V/V_{CC}$

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

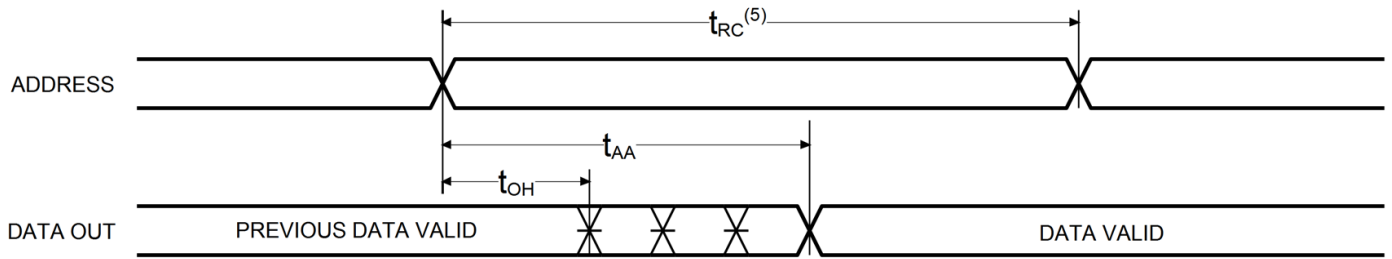
Sym	Parameter	-55		-70		-100		Unit
		Min	Max	Min	Max	Min	Max	
t _{RC}	Read Cycle Time	55		70		100		ns
t _{AA}	Address Access Time		55		70		100	ns
t _{AC}	Chip Enable Access Time		55		70		100	ns
t _{OH}	Output Hold from Address Change	5		5		5		ns
t _{LZ}	Chip Enable to Output in Low Z	10		10		10		ns
t _{HZ}	Chip Disable to Output in High Z		20		25		30	ns
t _{OE}	Output Enable Low to Data Valid		30		35		40	ns
t _{OLZ}	Output Enable Low to Low Z	5		5		5		ns
t _{OHZ}	Output Enable High to High Z		20		25		30	ns
t _{PU}	Chip Enable to Power Up Time	0		0		0		ns
t _{PD}	Chip Disable to Power Down		55		70		100	ns

TIMING WAVEFORM OF READ CYCLE NO. 1 (\overline{OE} CONTROLLED)⁽¹⁾

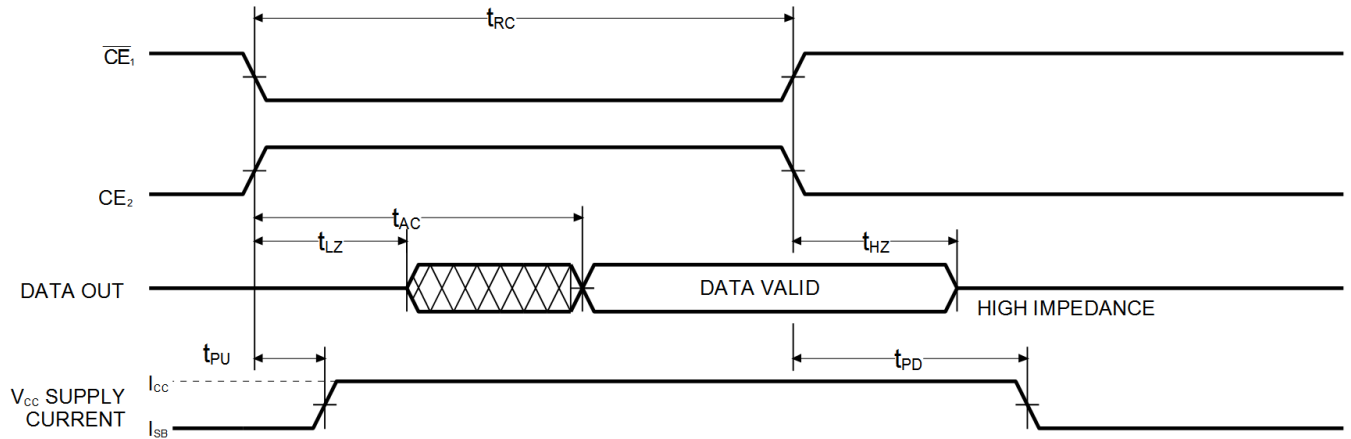




TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)



TIMING WAVEFORM OF READ CYCLE NO. 3 (CE CONTROLLED)



Notes:

1. \overline{WE} is HIGH for READ cycle.
2. \overline{CE}_1 and \overline{OE} are LOW, and CE_2 is HIGH for READ cycle.
3. ADDRESS must be valid prior to, or coincident with later of \overline{CE}_1 transition LOW or CE_2 transition HIGH.
4. Transition is measured ± 200 mV from steady state voltage prior to

- change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
5. READ Cycle Time is measured from the last valid address to the first transitioning address.

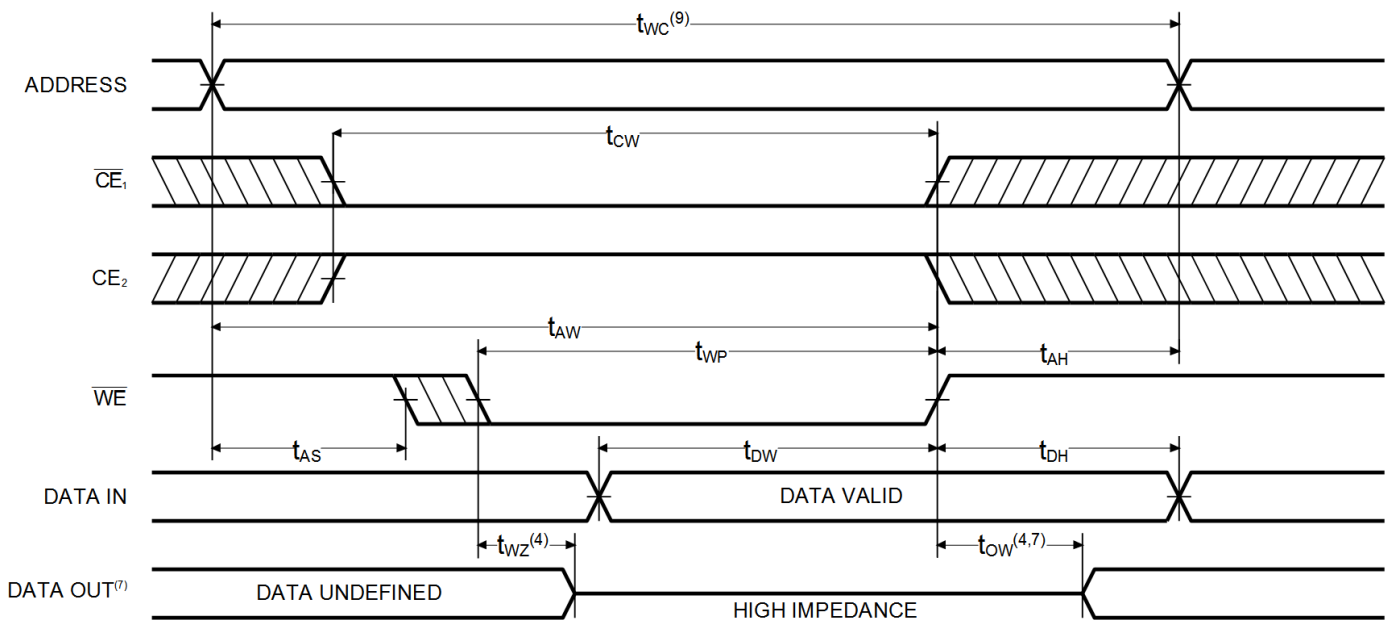


AC CHARACTERISTICS—WRITE CYCLE

($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Sym	Parameter	-55		-70		-100		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	55		70		100		ns
t_{CW}	Chip Enable Time to End of Write	50		60		75		ns
t_{AW}	Address Valid to End of Write	50		60		75		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	40		50		60		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{DW}	Data Valid to End of Write	25		30		35		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		25		30		35	ns
t_{OW}	Output Active from End of Write	5		5		5		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)⁽⁶⁾

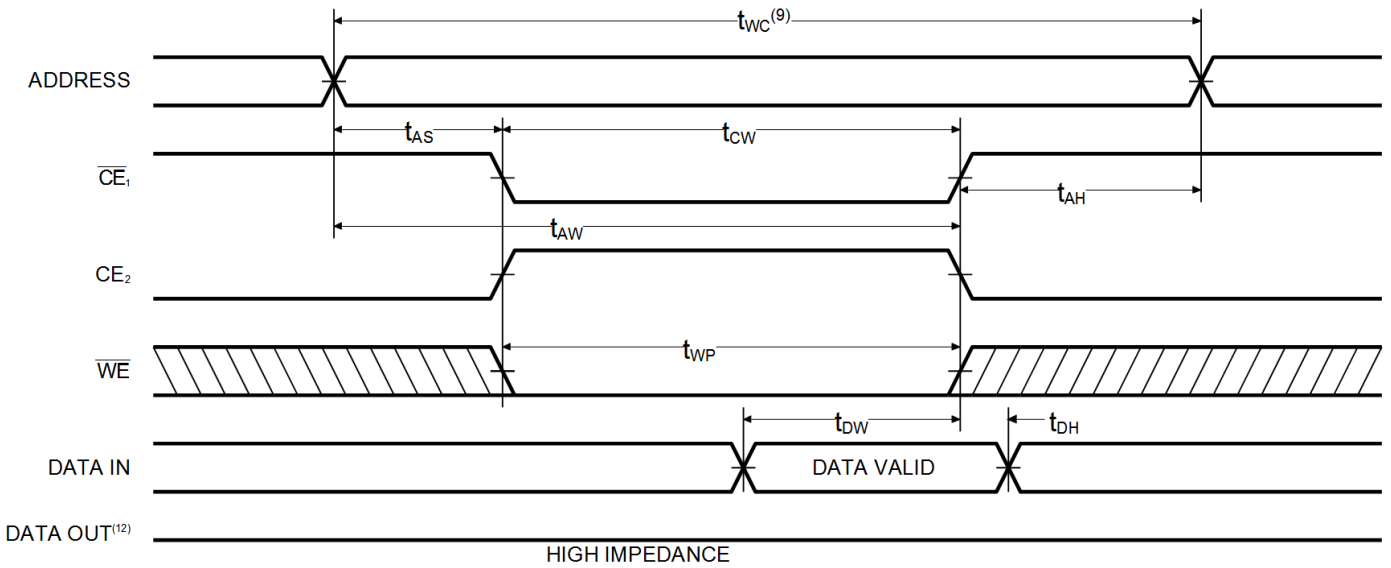


Notes:

- \overline{CE}_1 and \overline{WE} are LOW and CE_2 is HIGH for WRITE cycle.
- \overline{OE} is LOW for this WRITE cycle to show t_{WZ} and t_{OW} .
- If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in a high impedance state.
- Write Cycle Time is measured from the last valid address to the first transitioning address.



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CE} CONTROLLED)⁽⁶⁾



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	\overline{CE}_1	CE_2	\overline{OE}	\overline{WE}	I/O	Power
Standby	H	H	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	High Z	Active

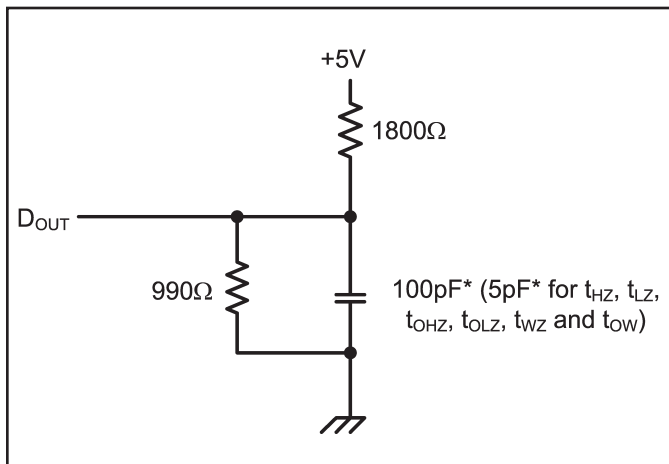


Figure 1. Output Load

* including scope and test fixture.

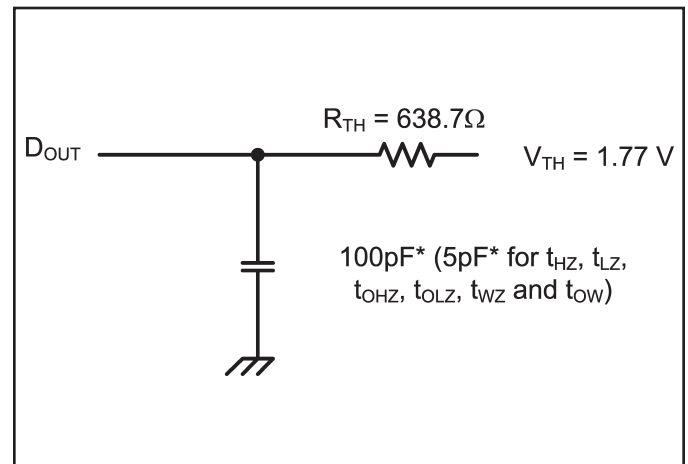


Figure 2. Thevenin Equivalent

Note:

Because of the ultra-high speed of the P4C1024L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μ F high frequency capacitor

is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.77V (Thevenin Voltage) at the comparator input, and a 589 Ω resistor must be used in series with D_{OUT} to match 639 Ω (Thevenin Resistance).

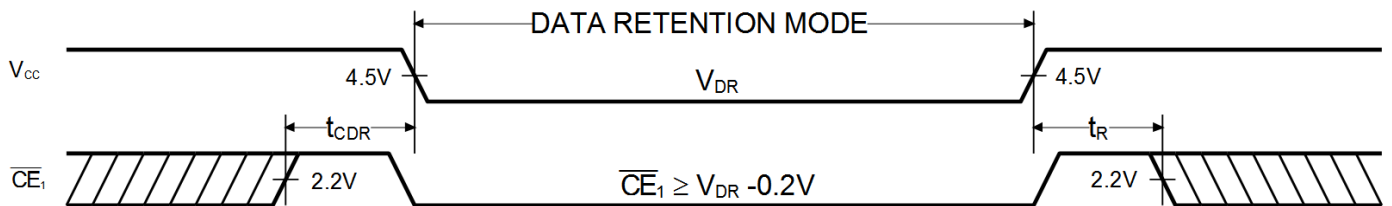
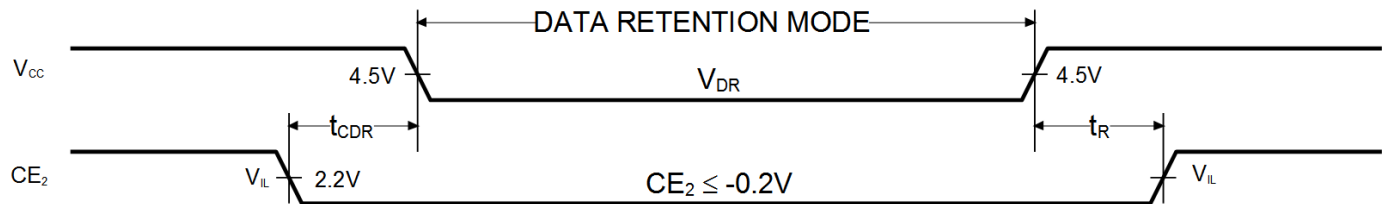
**DATA RETENTION CHARACTERISTICS**

Sym	Parameter	Test Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	$CE_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	5.5	V
$I_{CCDR}^{(1)}$	Data Retention Current	$V_{DR} = 2.0V$		75	μA
		$V_{DR} = 3.0V$		100	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0		ns

1. $\overline{CE}_1 \leq 0.2V$, $CE_2 \leq 0.2V$ or $\overline{CE}_1 \geq V_{DR} - 0.2V$, $CE_2 \leq 0.2V$ or $\overline{CE}_1 \geq V_{DR} - 0.2V$, $CE_2 \geq V_{DR} - 0.2V$

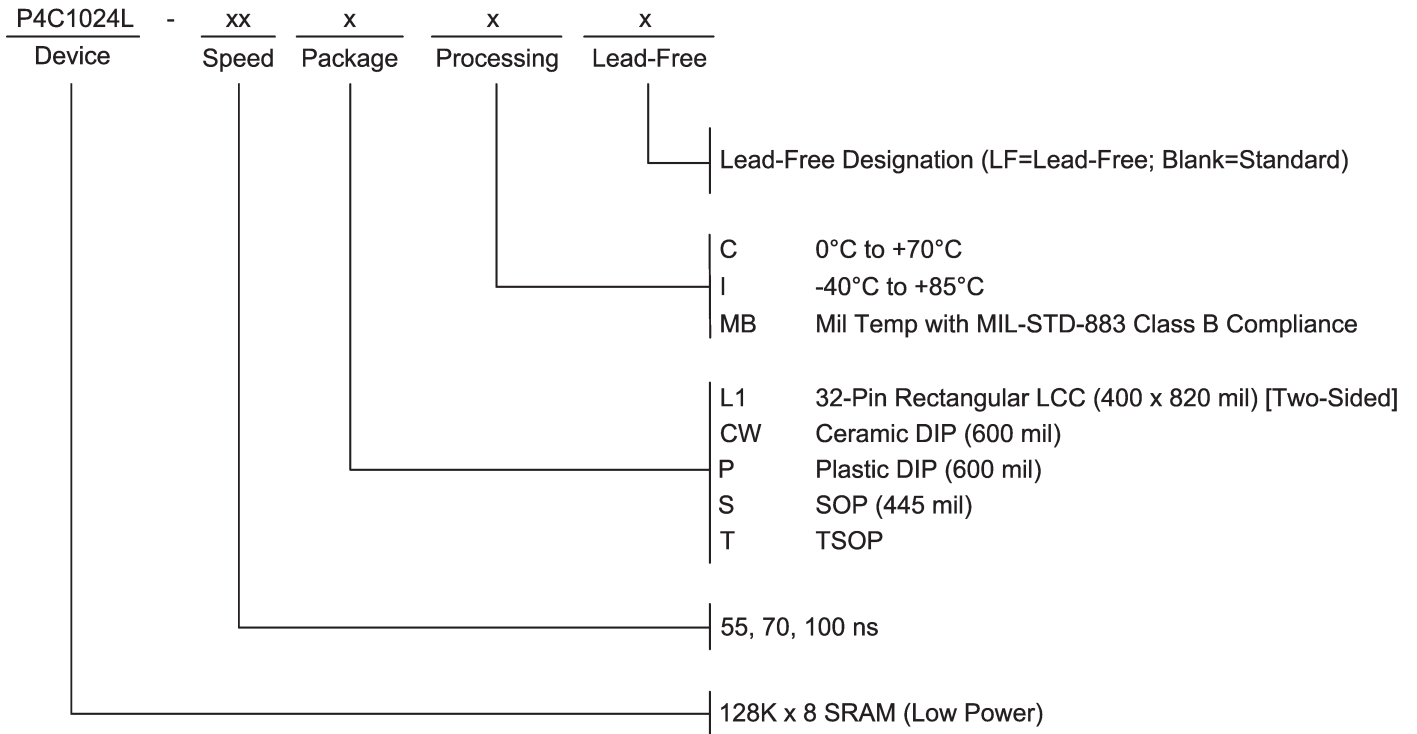
AND

$V_{IN} \geq V_{DR} - 0.2V$ or $V_{IN} \leq 0.2V$

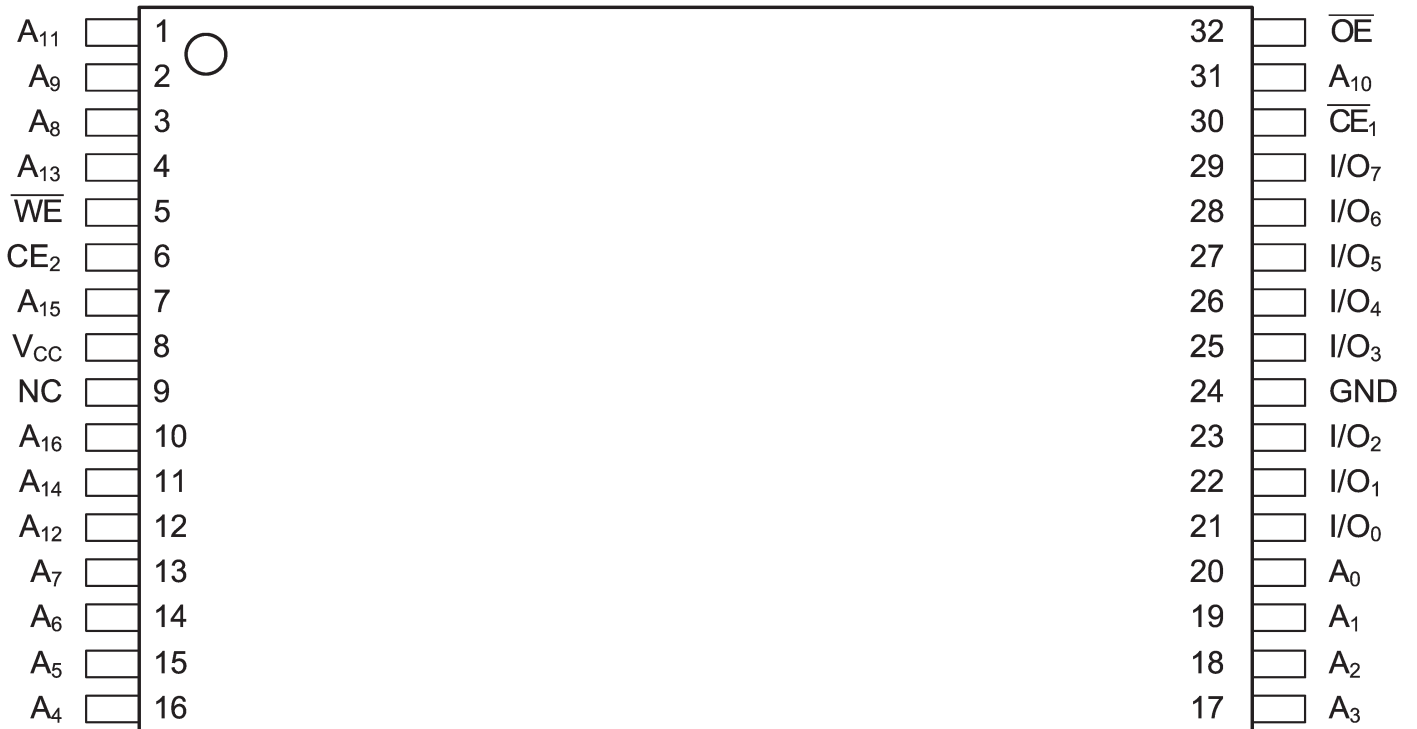
LOW V_{CC} DATA RETENTION WAVEFORM 1 (\overline{CE}_1 CONTROLLED)**LOW V_{CC} DATA RETENTION WAVEFORM 2 (CE_2 CONTROLLED)**



ORDERING INFORMATION



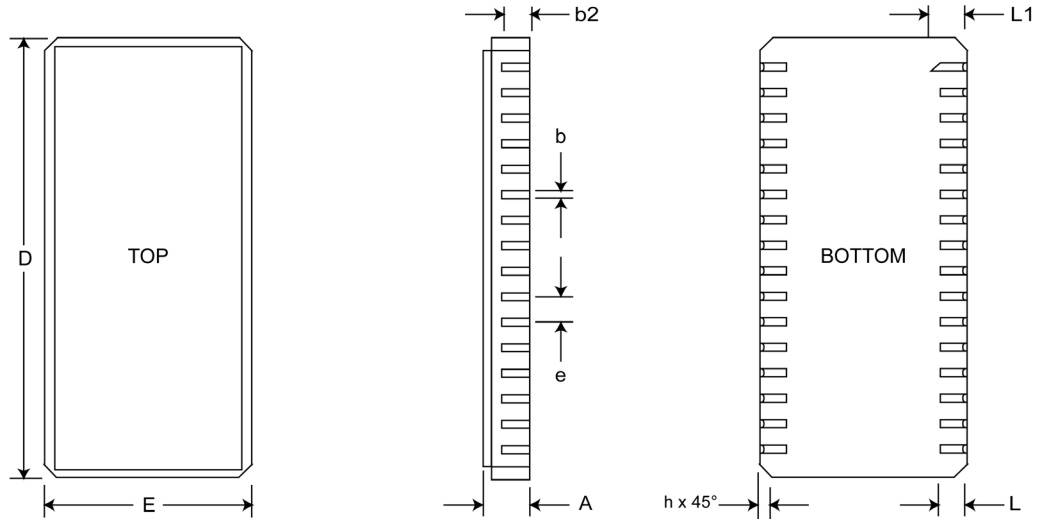
TSOP PIN CONFIGURATION





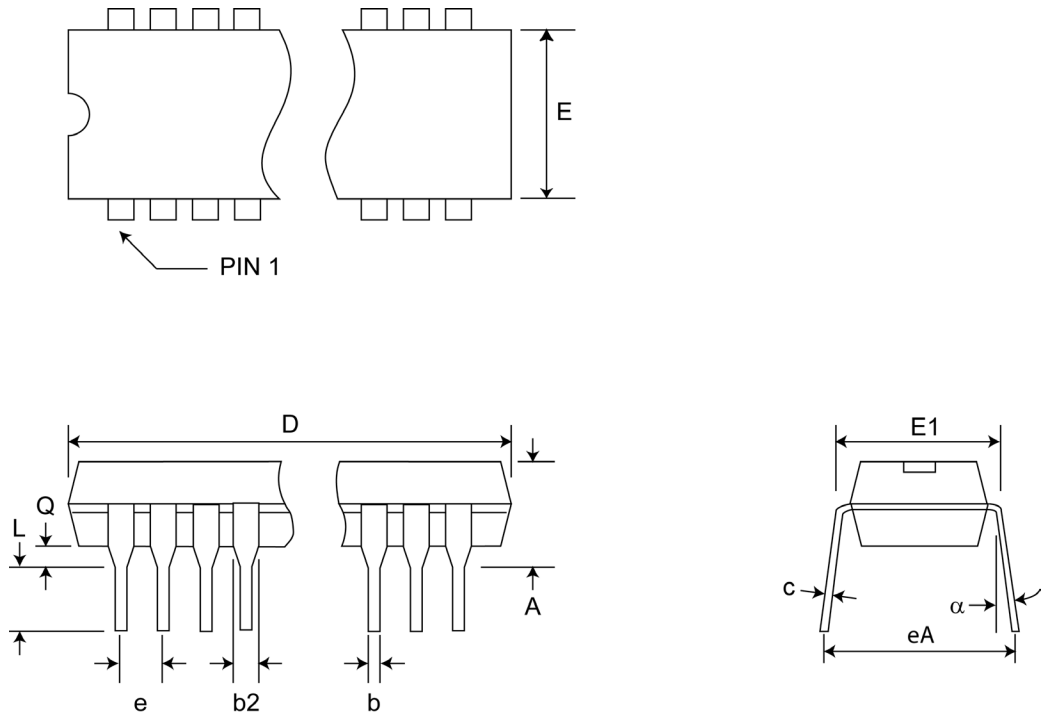
Pkg #	L1	
# Pins	32	
Symbol	Min	Max
A	0.080	0.100
b	0.022	0.028
b1	0.006	0.022
b2	0.040	-
D	0.800	0.840
E	0.392	0.400
e	0.050 BSC	
h	0.012 REF	
L	0.070	0.080
L1	0.090	0.110
L2	0.003	0.015
N	32	

RECTANGULAR LEADLESS CHIP CARRIER [TWO-SIDED]



Pkg #	P600	
# Pins	32 (600 mil)	
Symbol	Min	Max
A	0.160	0.200
A1	0.015	-
b	0.014	0.023
b2	0.045	0.070
C	0.006	0.014
D	1.600	1.700
E1	0.526	0.548
E	0.590	0.610
e	0.100 BSC	
eB	0.600 BSC	
L	0.120	0.150
α	0°	15°

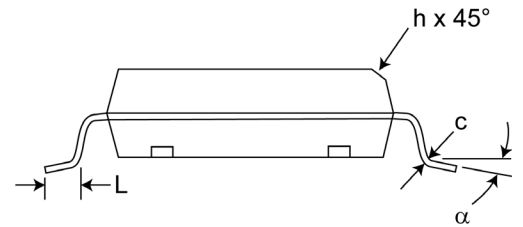
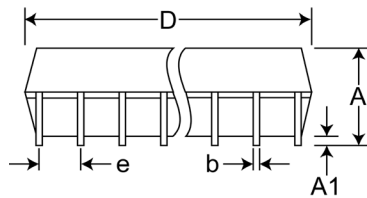
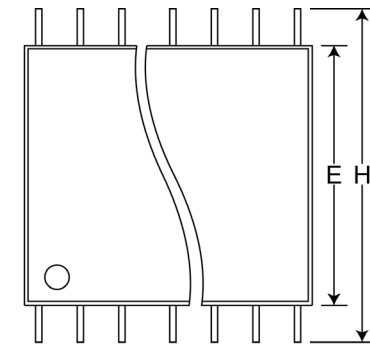
PLASTIC DUAL IN-LINE PACKAGE





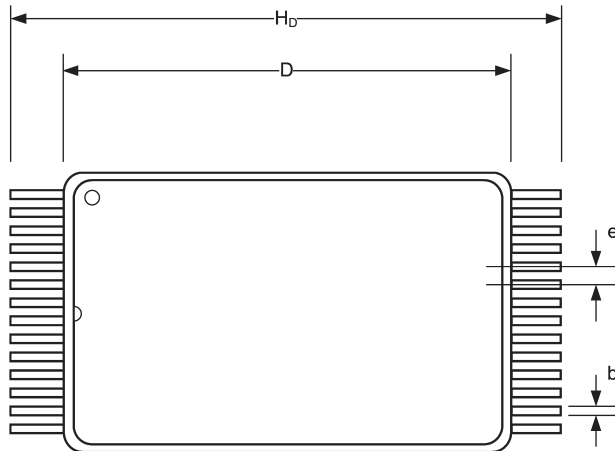
Pkg #	S12	
# Pins	32 (445 Mil)	
Symbol	Min	Max
A	-	0.118
A1	0.004	-
A2	0.101	0.111
B	0.014	0.020
C	0.006	0.012
D	0.793	0.817
e	0.050 BSC	
E	0.440	0.450
H	0.546	0.566
L	0.023	0.039
L1	0.047	0.063
α	0°	4°

SOIC/SOP SMALL OUTLINE IC PACKAGE

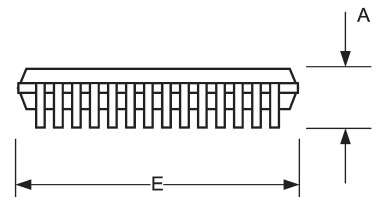


Pkg #	T3	
# Pins	32	
Symbol	Min	Max
A	-	0.048
A ₂	0.037	0.042
b	0.006	0.011
D	0.720	0.729
E	0.307	0.323
e	0.50 mm BSC	
H _D	0.779	0.796

TSOP THIN SMALL OUTLINE PACKAGE (8 x 20 mm)



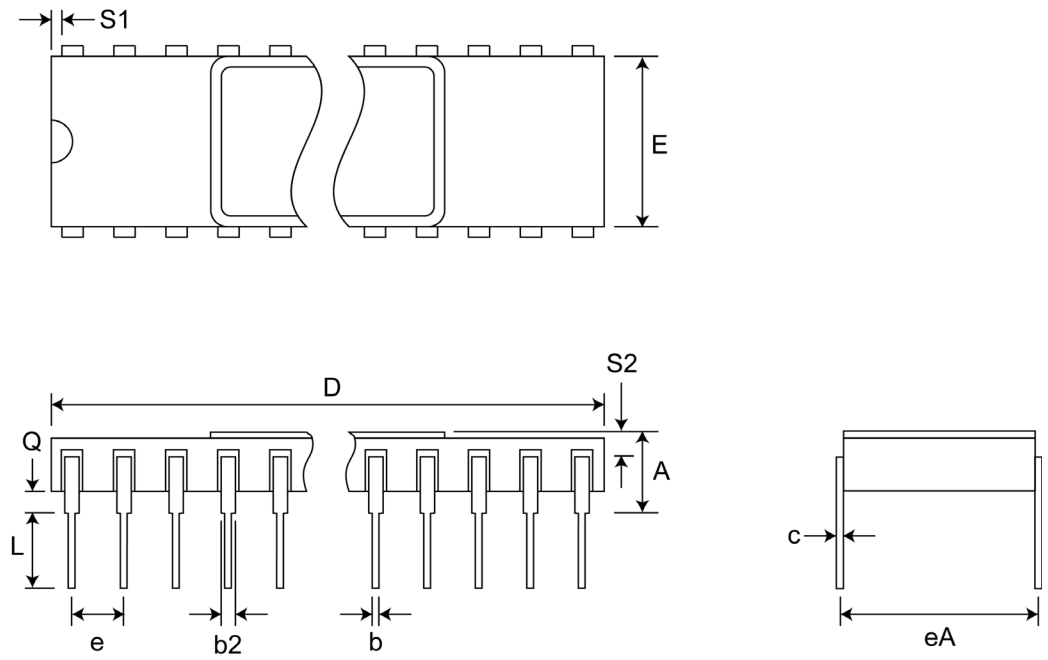
NOTE:
Orientation ID is either next to Pin 1 (midway along row of pins) or in corner on side of package containing Pin 1.





Pkg #	C10	
# Pins	32 (600 mil)	
Symbol	Min	Max
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.680
E	0.510	0.620
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



**REVISIONS**

DOCUMENT NUMBER	SRAM 125
DOCUMENT TITLE	P4C1024L - LOW POWER 128K x 8 CMOS STATIC RAM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-2005	JDB	Changed logo to Pyramid
B	Feb-2006	JDB	Added TSOP package
C	Sep-2006	JDB	Added Ceramic DIP package
D	May-2007	JDB	Corrected errors in P600 package dimensions
E	Nov-2008	JDB	Added L1 package, lead-free option
F	Nov-2008	JDB	Changed layout and formatting, no significant changes to content
G	Sep-2010	JDB	Corrected error in DC Electrical Characteristics table
H	May-2011	JDB	Added 100 ns speed