PYRAMID SEMICONDUCTOR CORPORATION

P4C116/P4C116L

ULTRA HIGH SPEED 2K X 8 STATIC CMOS RAMS

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 10/12/15/20/25/35 ns (Commercial)**
  - **– 12/15/20/25/35 ns (Industrial)**
  - **– 15/20/25/35 ns (Military)**
- **Low Power Operation**
- **Output Enable Control Function**
- **Single 5V±10% Power Supply**
- **Common Data I/O**
- **Fully TTL Compatible Inputs and Outputs**
- **Produced with PACE II Technology™**
- **Standard Pinout (JEDEC Approved)**
  - **– 24-Pin 300 mil DIP, SOIC, SOJ**
  - **– 24-Pin 600 mil DIP**
  - **– 24-Pin Solder Seal Flat Pack**
  - **– 24-Pin Rectangular LCC (300 x 400 mils)**
  - **– 28-Pin Square LCC (450 x 450 mils)**
  - **– 32-Pin Rectangular LCC (450 x 550 mils)**
  - **– 40-Pin Square LCC (480 x 480 mils)**

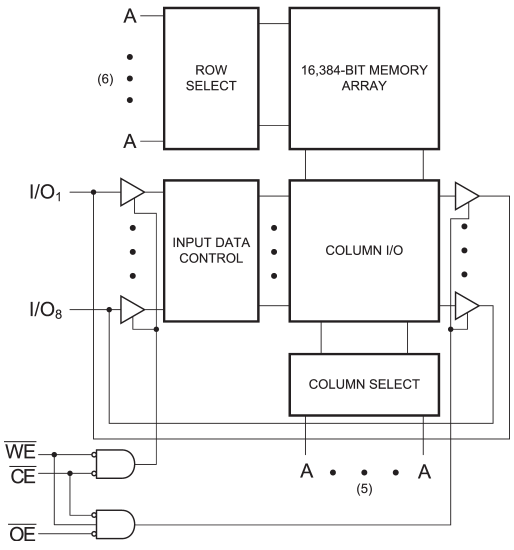
DESCRIPTION

The P4C116/P4C116L are 16,384-bit ultra high-speed static RAMs organized as 2K x 8. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V±10% tolerance power supply. Current drain is typically 10 µA from a 2.0V supply.

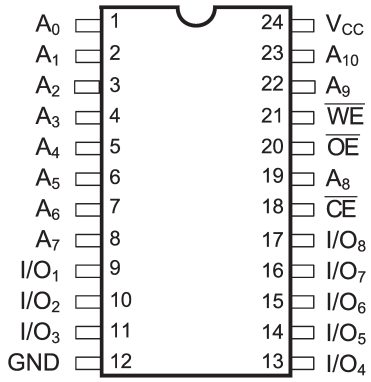
Access times as fast as 10 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption.

The P4C116 is available in 24-pin 300 and 600 mil DIP, SOJ and SOIC packages, a solder seal flatpack and 4 different LCC packages (24, 28, 32, and 40 pin).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (C4, C12, D4, P4), SOJ (J4), SOIC (S4)
SOLDER SEAL FLAT PACK (FS-1) SIMILAR

LCC configurations at end of datasheet

MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to VCC + 0.5	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{cc}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	7	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions		P4C116		P4C116L		Unit
				Min	Max	Min	Max	
V_{IH}	Input High Voltage			2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage			-0.5[3]	0.8	-0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC} - 0.2	V_{CC} + 0.5	V_{CC} - 0.2	V_{CC} + 0.5	V
V_{LC}	CMOS Input Low Voltage			-0.5[3]	0.2	-0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = -18 mA			-1.2		-1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min			0.4		0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = - 4 mA, V_{CC} = Min		2.4		2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = GND to V_{CC}	MIL	-10	+10	-5	+5	µA
			IND/COM	-5	+5	N/A	N/A	
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL	-10	+10	-5	+5	µA
			IND/COM	-5	+5	N/A	N/A	
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max, f = Max, Outputs Open	MIL	—	30	—	20	mA
			IND/COM	—	20	—	N/A	
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max, f = 0, Outputs Open V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	MIL	—	15	—	1	mA
			IND/COM	—	10	—	N/A	

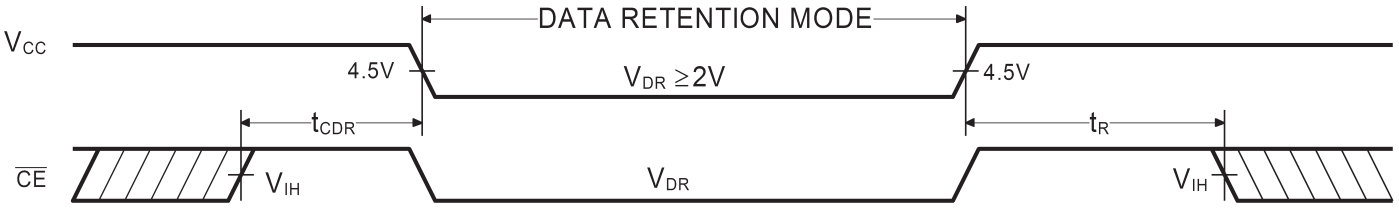
N/A = Not applicable

DATA RETENTION CHARACTERISTICS (P4C116L Military Temperature Only)

Sym	Parameter	Test Conditions	Min	Typ* V_{CC}=		Max V_{CC}=		Unit
				2.0V	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		10	15	600	900	µA
t_{CDR}	Chip Deselect to Data Retention Time		0					ns
t_R†	Operation Recovery Time		t_{RC}§					ns

* T_A = +25°C
§ t_{RC} = Read Cycle Time
† This Parameter is guaranteed but not tested

DATA RETENTION WAVEFORM



POWER DISSIPATION CHARACTERISTICS VS. SPEED

Sym	Parameter	Temperature Range	-10	-12	-15	-20	-25	-35	Unit
I_{CC}	Dynamic Operating Current*	Commercial	180	170	160	155	150	140	mA
		Industrial	N/A	180	170	160	155	150	mA
		Military	N/A	N/A	170	160	155	150	mA

* V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

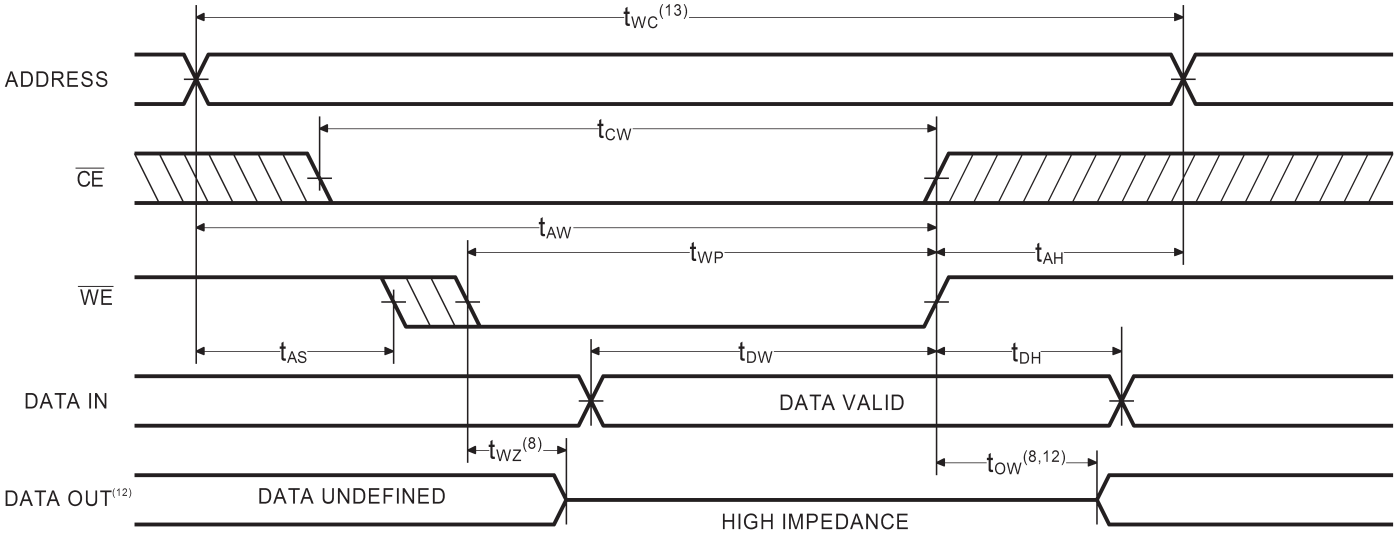
Sym	Parameter	-10		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	10		12		15		20		25		35		ns
t_{AA}	Address Access Time		10		12		15		20		25		35	ns
t_{AC}	Chip Enable Access Time		10		12		15		20		25		35	ns
t_{OH}	Output Hold from Address Change	2		2		2		2		2		2		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		5		6		7		8		10		15	ns
t_{OE}	Output Enable Low to Data Valid		6		8		10		10		15		20	ns
t_{OLZ}	Output Enable Low to Low Z	0		0		0		0		0		0		ns
t_{OHZ}	Output Enable High to High Z		6		7		8		9		12		15	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down		10		12		15		20		20		25	ns

AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

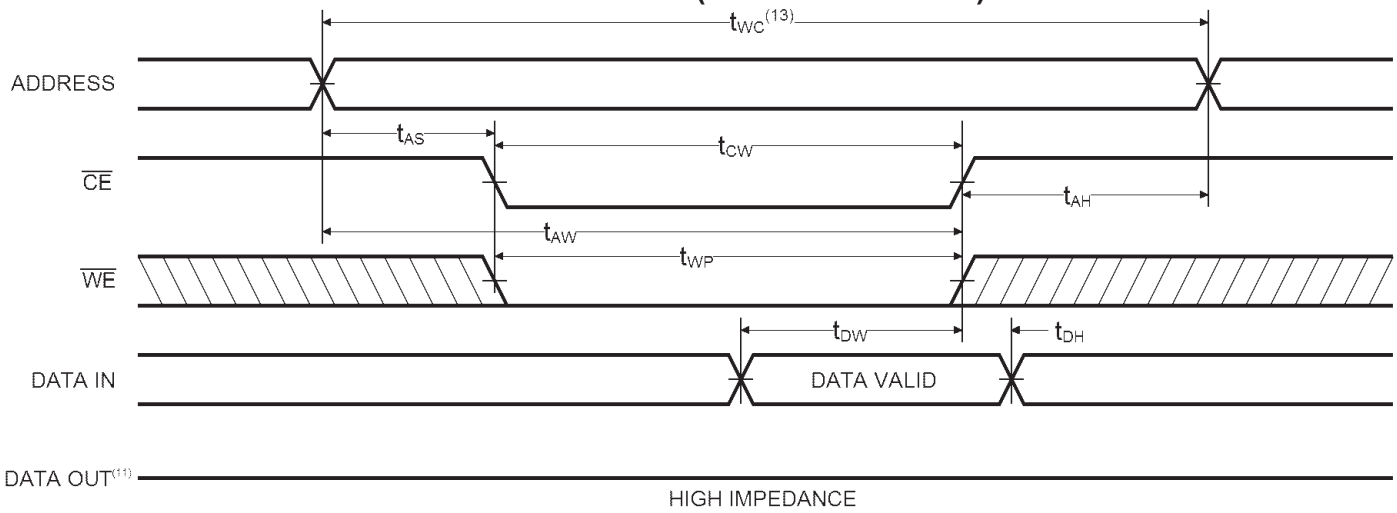
Sym	Parameter	-10		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	10		12		15		20		25		35		ns
t_{CW}	Chip Enable Time to End of Write	8		10		12		15		18		25		ns
t_{AW}	Address Valid to End of Write	8		10		12		15		18		25		ns
t_{AS}	Address Setup Time	0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	8		10		12		15		18		20		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	7		8		10		12		15		20		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		6		7		8		10		15		15	ns
t_{OW}	Output Active from End of Write	0		0		0		0		0		0		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[10,11]



Notes:
10. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
11. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state
13. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[10]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	High Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	High Z	Active

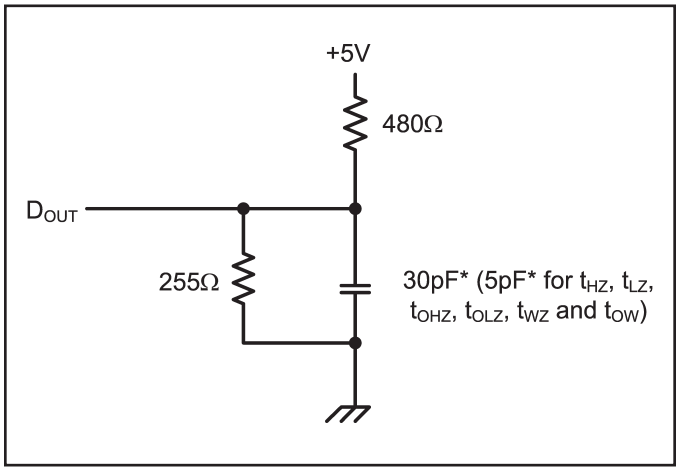


Figure 1. Output Load

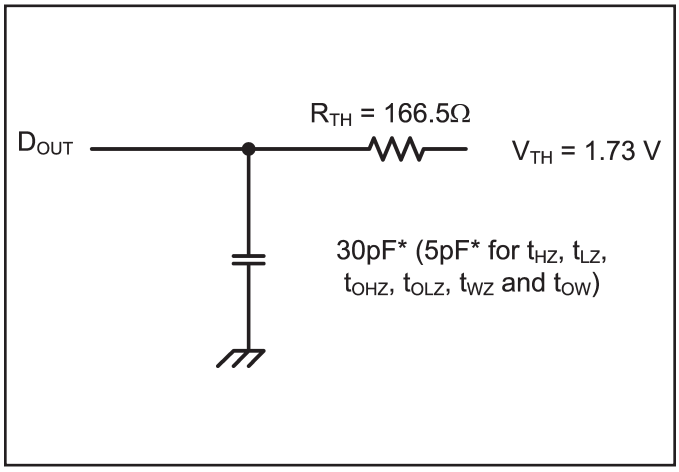
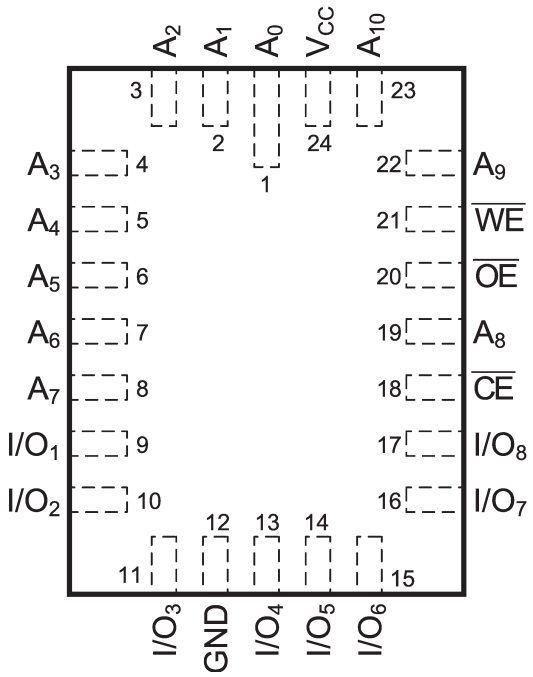


Figure 2. Thevenin Equivalent

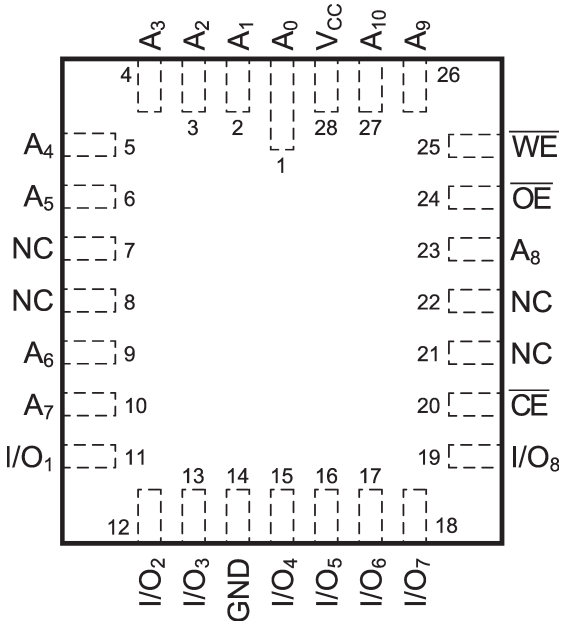
* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C116/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

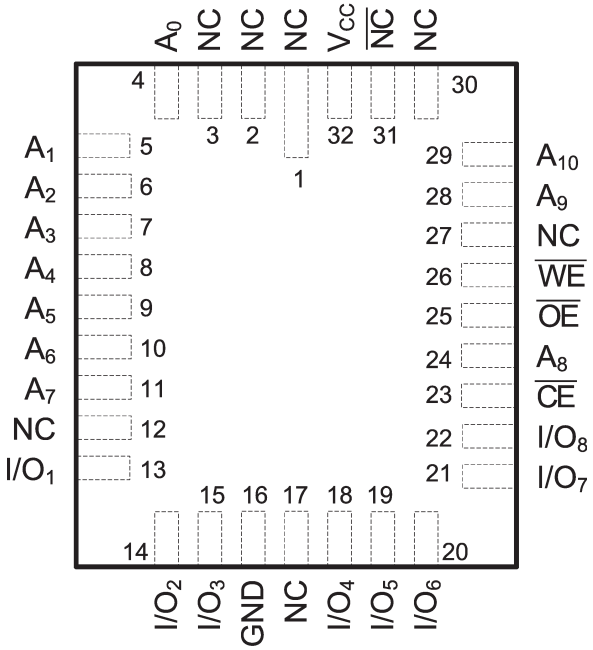
LCC PIN CONFIGURATIONS



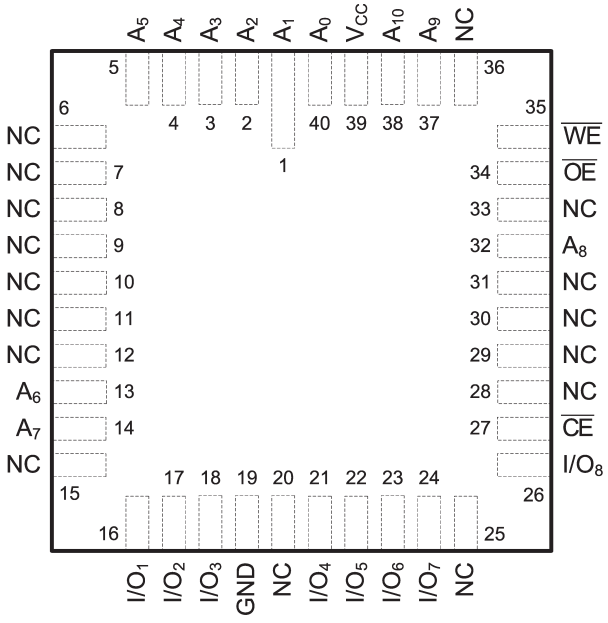
24-Pin LCC (L8)



28-Pin LCC (L5-1)

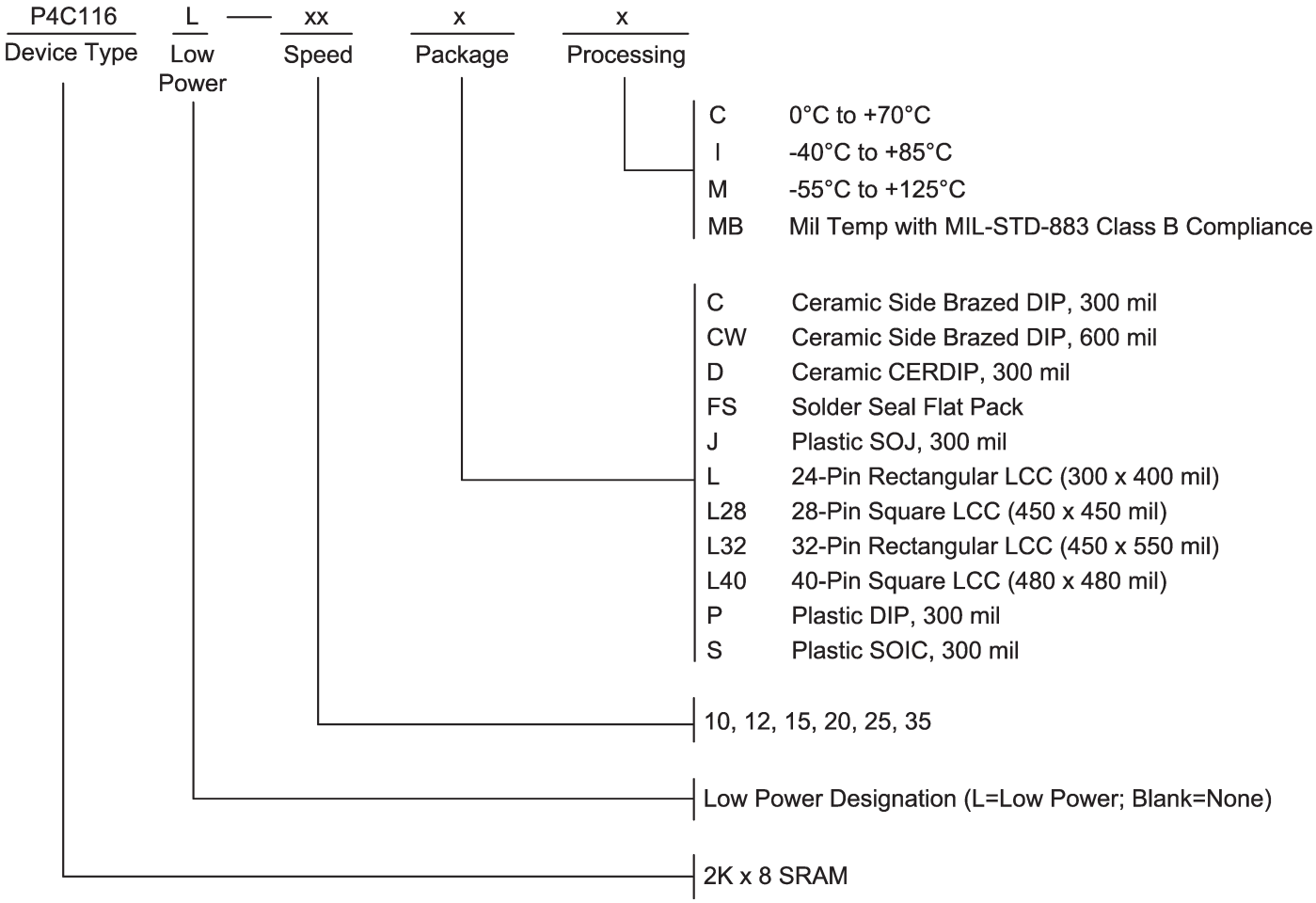


32-Pin LCC (L6)



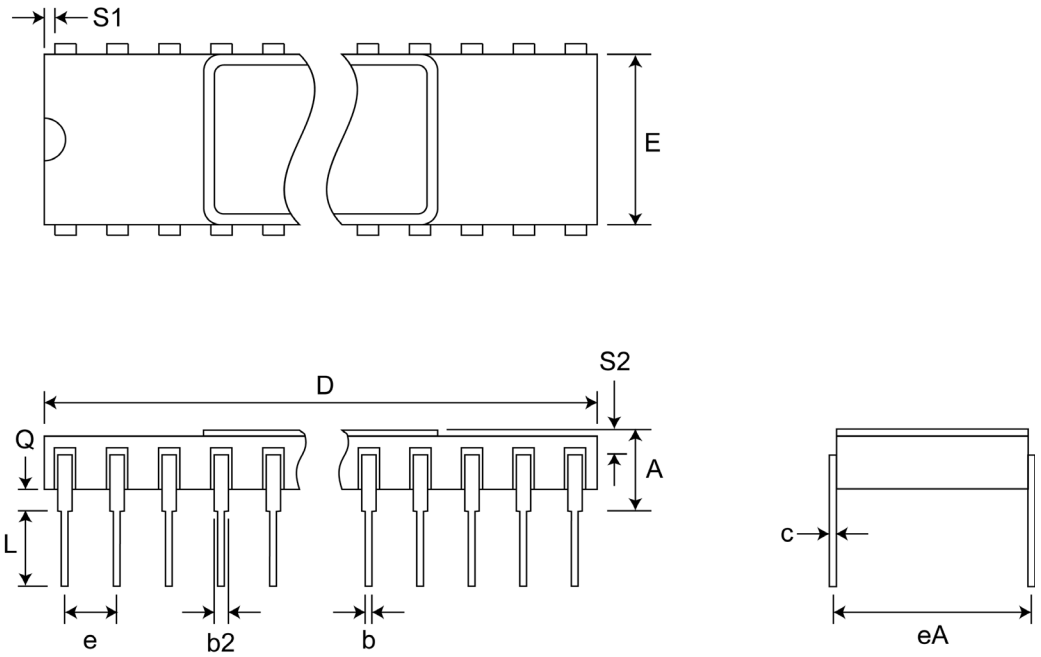
40-Pin LCC (L10)

ORDERING INFORMATION



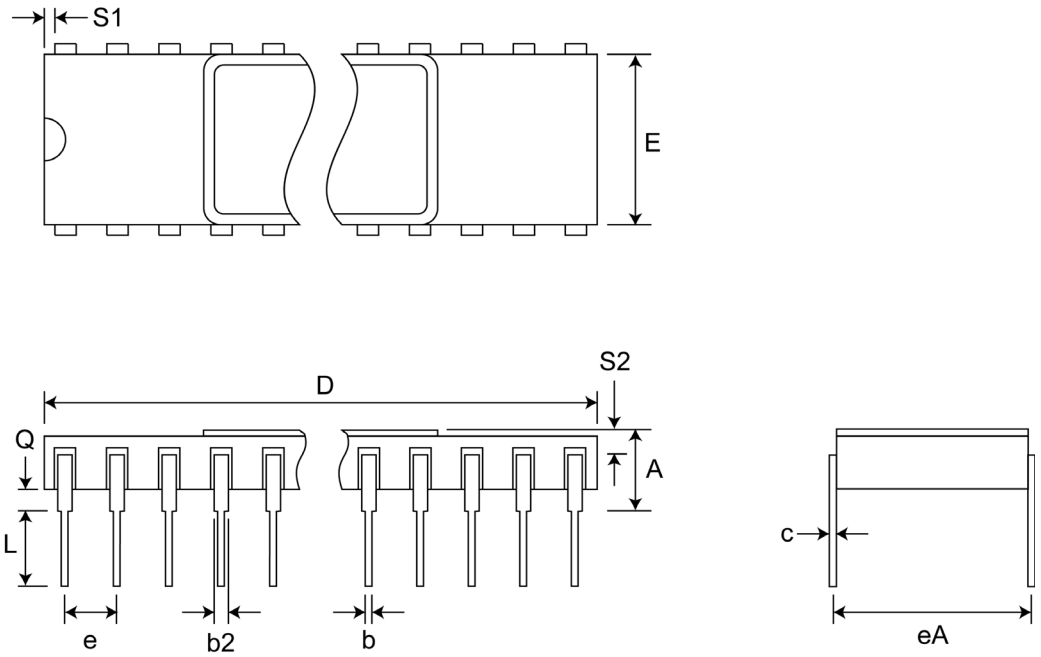
Pkg #	C4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



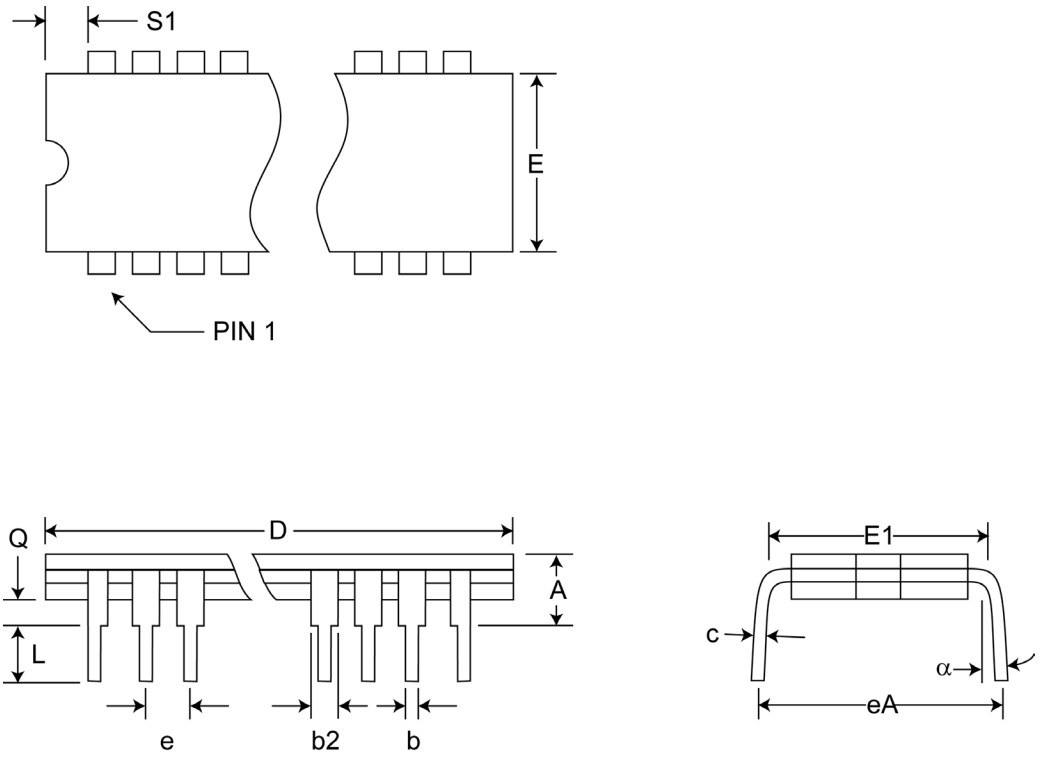
Pkg #	C12	
# Pins	24 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.232
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.290
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



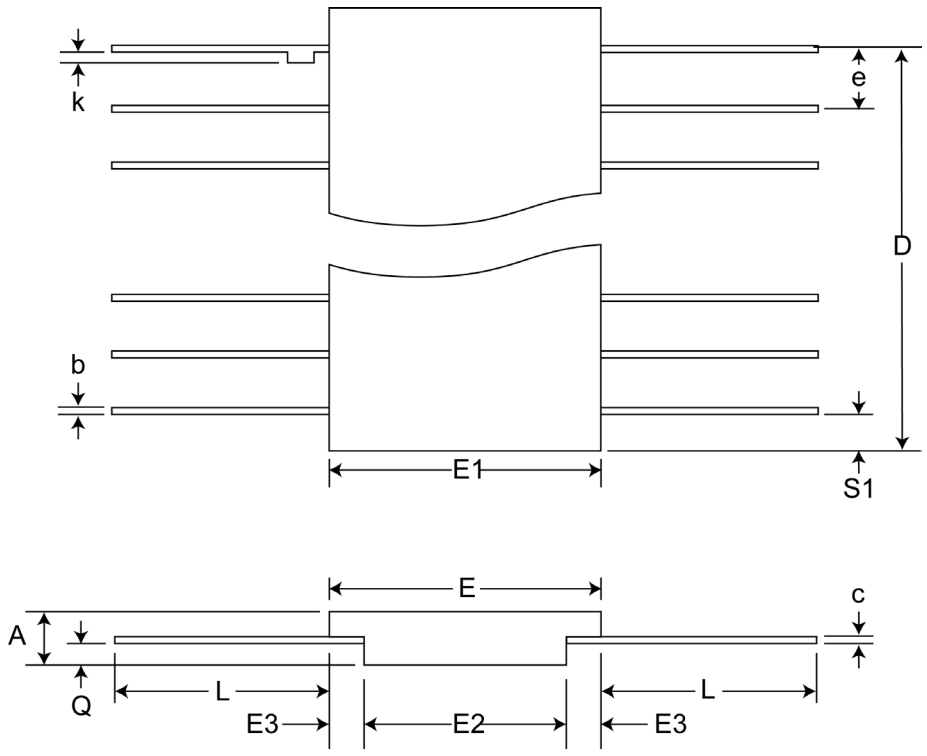
Pkg #	D4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0°	15°

CERDIP DUAL INLINE PACKAGE



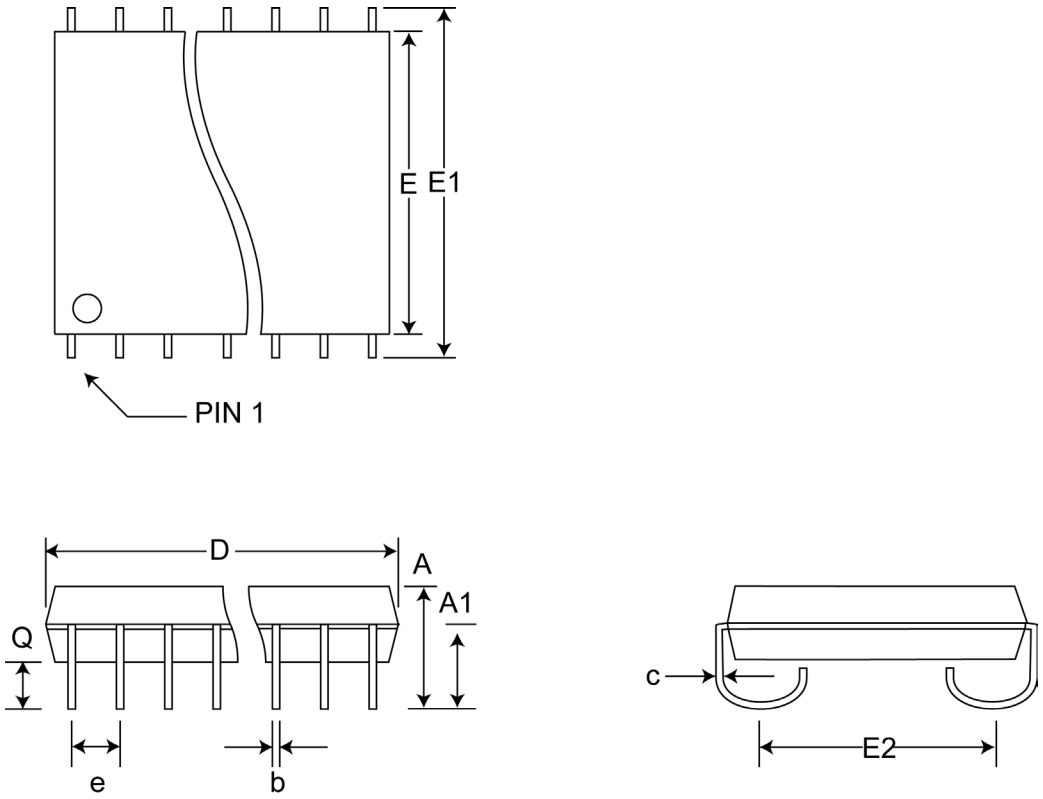
Pkg #	FS-1	
# Pins	24	
Symbol	**Min**	**Max**
A	0.045	0.115
b	0.015	0.022
b1	0.015	0.019
c	0.004	0.009
c1	0.004	0.006
D	-	0.640
E	0.350	0.420
E1	-	0.450
E2	0.180	-
E3	0.030	-
e	0.050 BSC	
k	0.008	0.015
L	0.250	0.370
Q	0.026	0.045
S1	0.000	-
M	-	0.002
N	24	

SOLDER SEAL FLATPACK



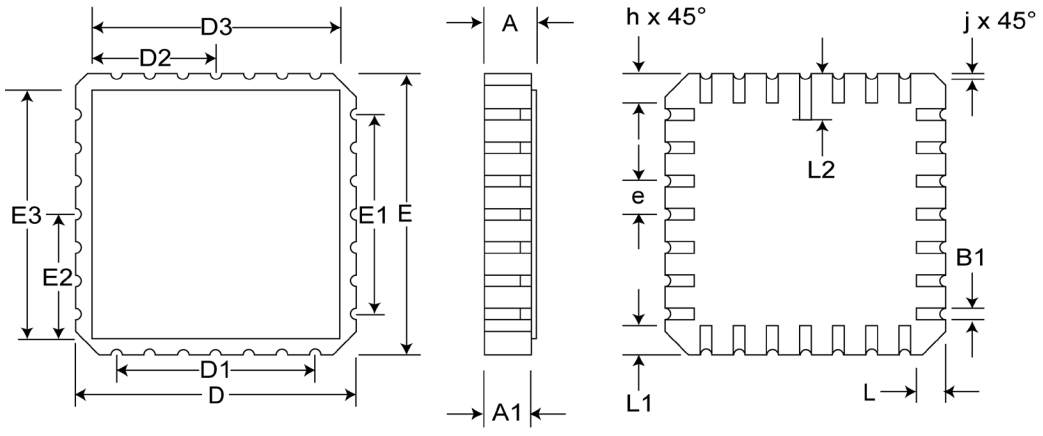
Pkg #	J4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.016	0.020
C	0.007	0.010
D	0.620	0.630
e	0.050 BSC	
E	0.335 BSC	
E1	0.292	0.300
E2	0.267 BSC	
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE



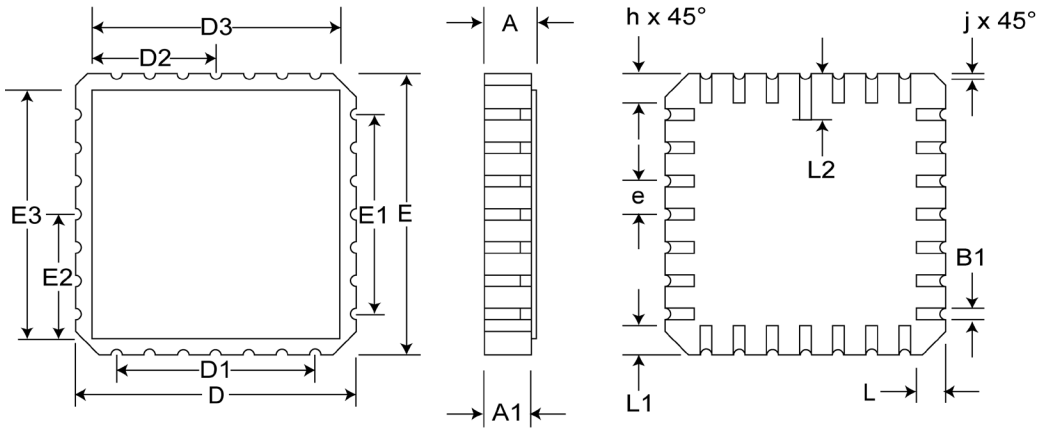
Pkg #	L5-1	
# Pins	28	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D/E	0.442	0.460
D1/E1	0.300 BSC	
D2/E2	0.150 BSC	
D3/E3	-	0.460
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	7	

SQUARE LEADLESS CHIP CARRIER



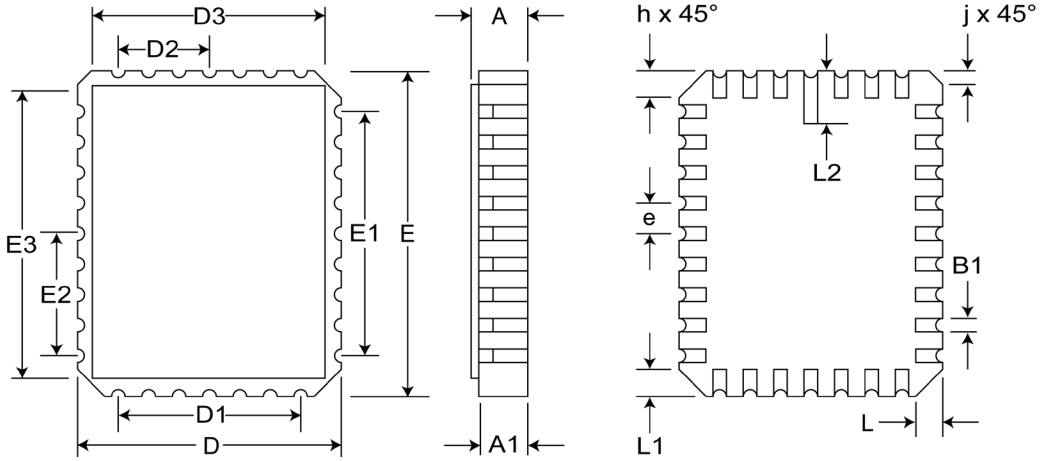
Pkg #	L10	
# Pins	40	
Symbol	**Min**	**Max**
A	0.060	0.080
A1	0.050	0.075
B1	0.015	0.025
D/E	0.475	0.492
D1/E1	0.360 BSC	
D2/E2	0.180 BSC	
D3/E3	-	0.492
e	0.040 BSC	
h	R = .0075	
j	0.026 REF	
L	0.030	0.050
L1	0.030	0.050
L2	0.080	0.090
ND	10	
NE	10	

SQUARE LEADLESS CHIP CARRIER



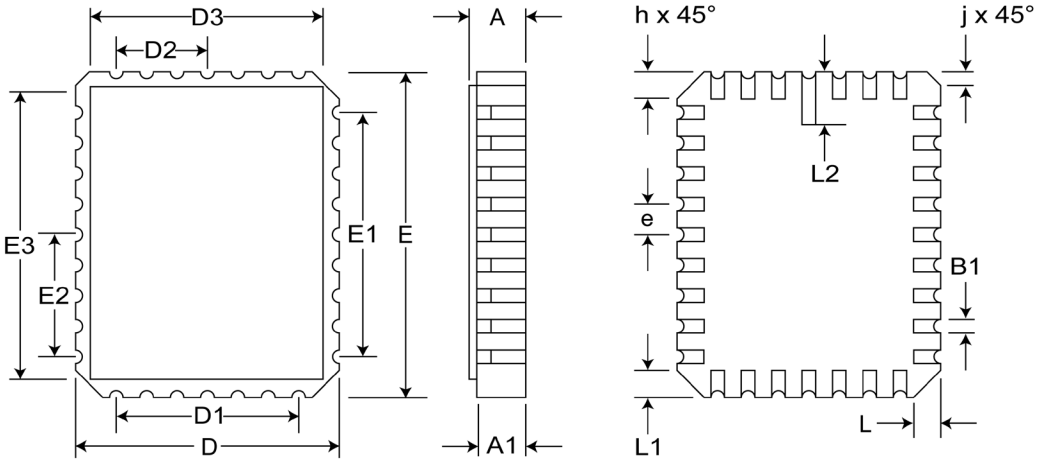
Pkg #	L6	
# Pins	32	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	-	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	

RECTANGULAR LEADLESS CHIP CARRIER



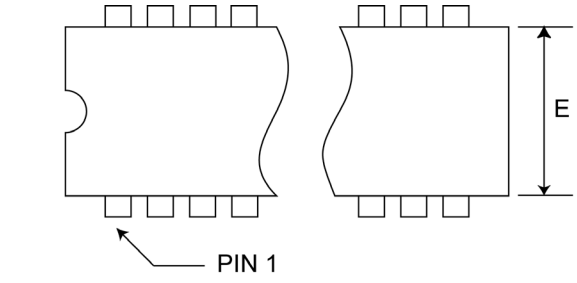
Pkg #	L8	
# Pins	24	
Symbol	**Min**	**Max**
A	0.064	0.076
A1	0.054	0.066
B1	0.022	0.028
D	0.292	0.308
D1	0.200 BSC	
D2	0.100 BSC	
D3	-	0.308
E	0.392	0.408
E1	0.300 BSC	
E2	0.150 BSC	
E3	-	0.408
e	0.050 BSC	
h	0.025 REF	
j	0.015 REF	
L	0.040	0.050
L1	0.040	0.050
L2	0.077	0.093
ND	5	
NE	7	

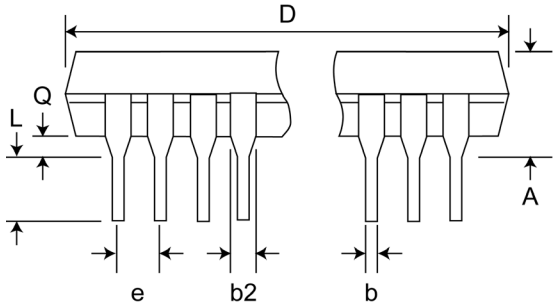
RECTANGULAR LEADLESS CHIP CARRIER

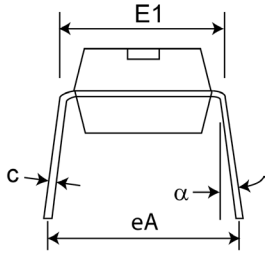


Pkg #	P4	
# Pins	24 (300 Mil)	
Symbol	**Min**	**Max**
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.070
C	0.008	0.014
D	1.230	1.280
E1	0.240	0.280
E	0.280	0.325
e	0.100 BSC	
eB	-	0.430
L	0.115	0.160
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE

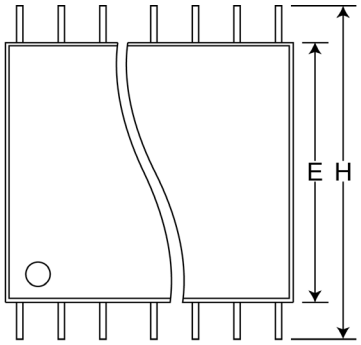


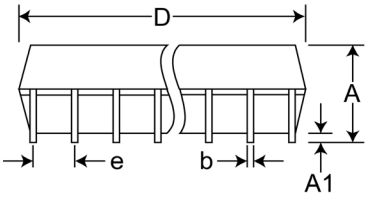


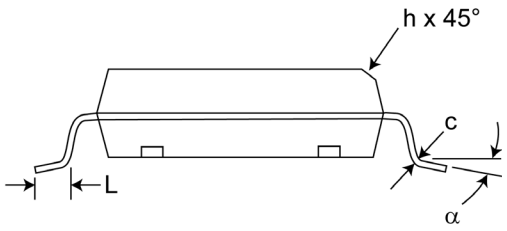


Pkg #	S4	
# Pins	24 (300 Mil)	
Symbol	**Min**	**Max**
A	0.093	0.104
A1	0.004	0.012
b2	0.013	0.020
C	0.009	0.012
D	0.598	0.614
e	0.050 BSC	
E	0.291	0.299
H	0.394	0.419
h	0.010	0.029
L	0.016	0.050
α	0°	8°

SOIC/SOP SMALL OUTLINE IC PACKAGE







REVISIONS

DOCUMENT NUMBER	SRAM 110
DOCUMENT TITLE	P4C116 / P4C116L ULTRA HIGH SPEED 2K X 8 STATIC CMOS RAMS

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-2005	JDB	Changed logo to Pyramid
B	Feb-2009	JDB	Added Industrial Temperature Range
C	May-2009	JDB	Added 300 mil CERDIP and 600 mil sidebrazed packages