P4C189
HIGH SPEED 16 x 4
STATIC CMOS RAM WITH INVERTING OUTPUTS

FEATURES

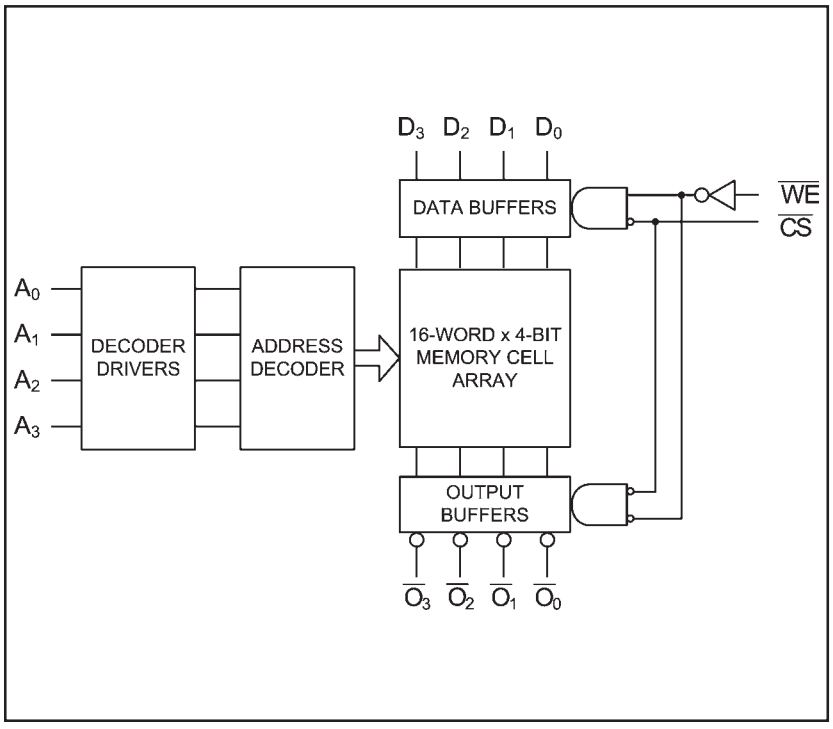
- **16 x 4 Static RAM**
- **Fast Access Time – 35 ns Commercial and Industrial**
- **Available in the following packages:**
  – 16-Pin PDIP
- **Inverted Outputs**
- **5V Power Supply ±10% for both commercial and industrial temperature ranges.**
- **Separate I/O**
- **Fully static operation with equal access and cycle times**
- **3-STATE outputs for data bus applications**

DESCRIPTION

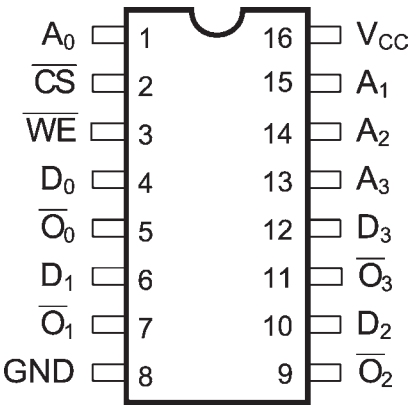
The P4C189 is a 64-bit high-speed Static RAM with a 16 x 4 organization. The memory requires no clocks or refreshing and has equal access and cycle times. Inputs and outputs are fully TTL compatible. Operation is from a single 5 Volt supply. The output data is the complement of the written data.

The P4C189 is offered in a 16-Pin DIP package. Devices are offered in both commercial and industrial temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP (P7)

MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	20	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	Gnd	Vcc
Commercial	0°C to 70°C	0V	5.0V ±10%
Industrial	–40°C to 85°C	0V	5.0V ±10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P4C189 Min.	P4C189 Max.	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = –3.0 mA		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 24 mA			0.5	V
V_{IH}	Input High Level			2.0		V
V_{IL}	Input Low Level				0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.5 V (except $\overline{CS}$)			-0.6	mA
		V_{IN} = 0.5 V ($\overline{CS}$)			-1.2	
I_{IH}	Input High Current	V_{CC} = Max, V_{IN} = 2.7V			5	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V		-150	-60	mA
I_{CC}	Power Supply Current	V_{CC} = Max.	Commercial		55	mA
			Industrial		70	
I_L	Output Leakage Current	V_{OUT} = V_{CC}, V_{CC} = Max.			50	µA

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.
5. $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{WE}$ is HIGH, and address must be valid prior to or coincident with $\overline{CE}$ transition LOW.
7. Transition is measured ±200mV from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.
8. Read Cycle Time is measured from the last valid address to the first transitioning address.

FUNCTIONAL DESCRIPTION

An active LOW write enable ($\overline{WE}$) controls the writing/reading operation of the memory. When chip select ($\overline{CS}$) and write enable ($\overline{WE}$) are LOW, the information on data inputs (D_0 through D_3) is written into the addressed memory word. Reading is performed with chip select ($\overline{CS}$) LOW and write enable ($\overline{WE}$) HIGH. The information stored in the addressed word is read out on the inverting outputs ($\overline{O}_0$ through $\overline{O}_3$). The outputs of the memory go to an inactive high impedance state whenever chip select ($\overline{CS}$) is HIGH, or during the write operation when write enable ($\overline{WE}$) is LOW.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output
Standby	H	X	High Z
Read	L	H	$\overline{D_{OUT}}$
Write	L	L	High Z

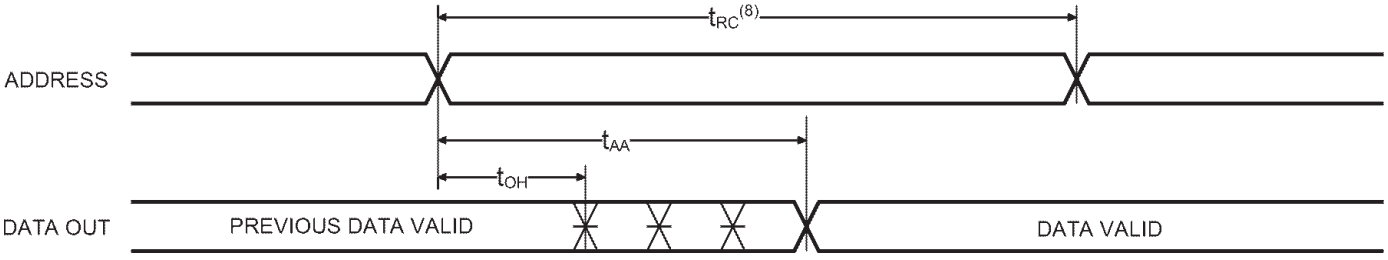
Notes: H = HIGH
L = Low
X = Don't Care
HIGH Z = Implies outputs are disabled or off. This condition is defined as high impedance state.

AC CHARACTERISTICS—READ CYCLE

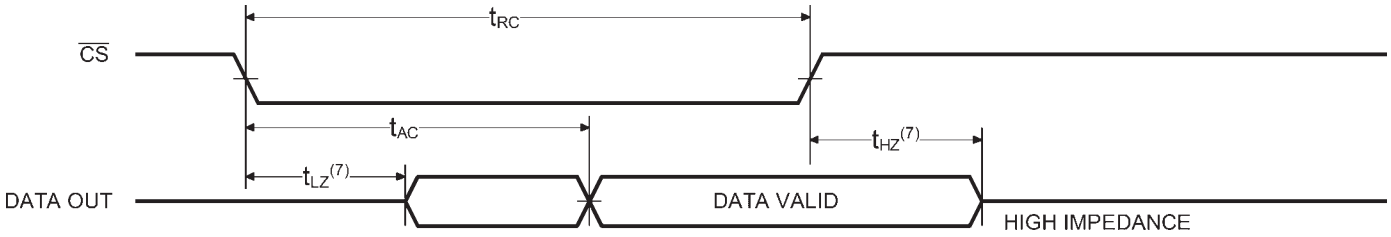
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-35		Unit
		Min	Max	
t_{RC}	Read Cycle Time	35		ns
t_{AA}	Address Access Time		35	ns
t_{AC}	Chip Enable Access Time		15	ns
t_{OH}	Output Hold from Address Change	2		ns
t_{LZ}	Chip Enable to Output in Low Z	2		ns
t_{HZ}	Chip Disable to Output in High Z		10	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[5]



TIMING WAVEFORM OF READ CYCLE NO. 2 (6)

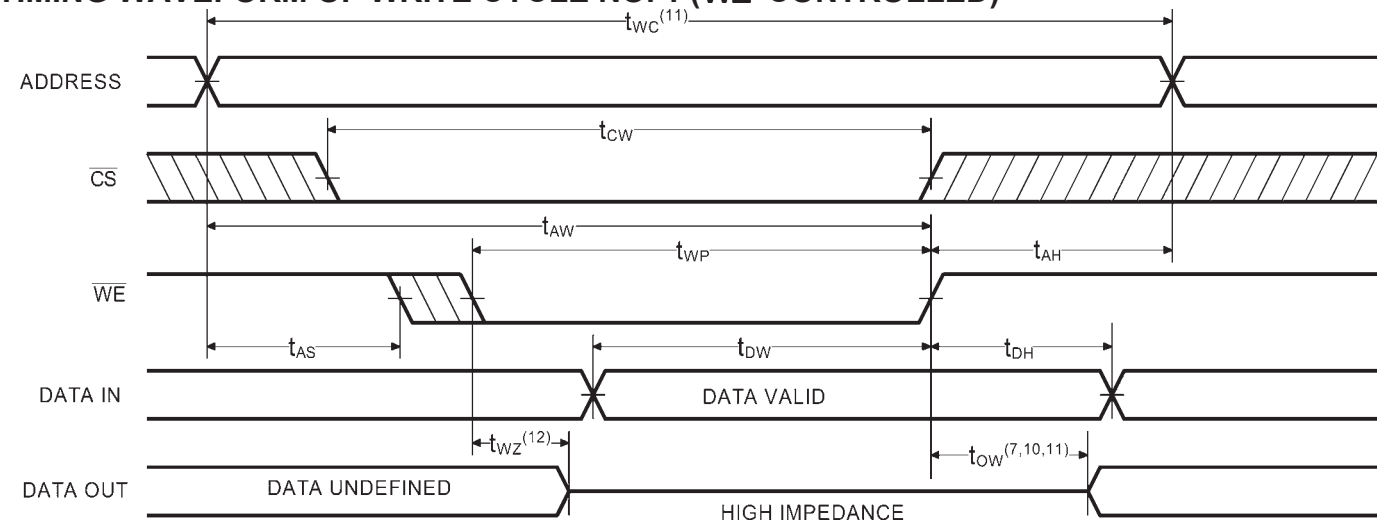


AC CHARACTERISTICS—WRITE CYCLE

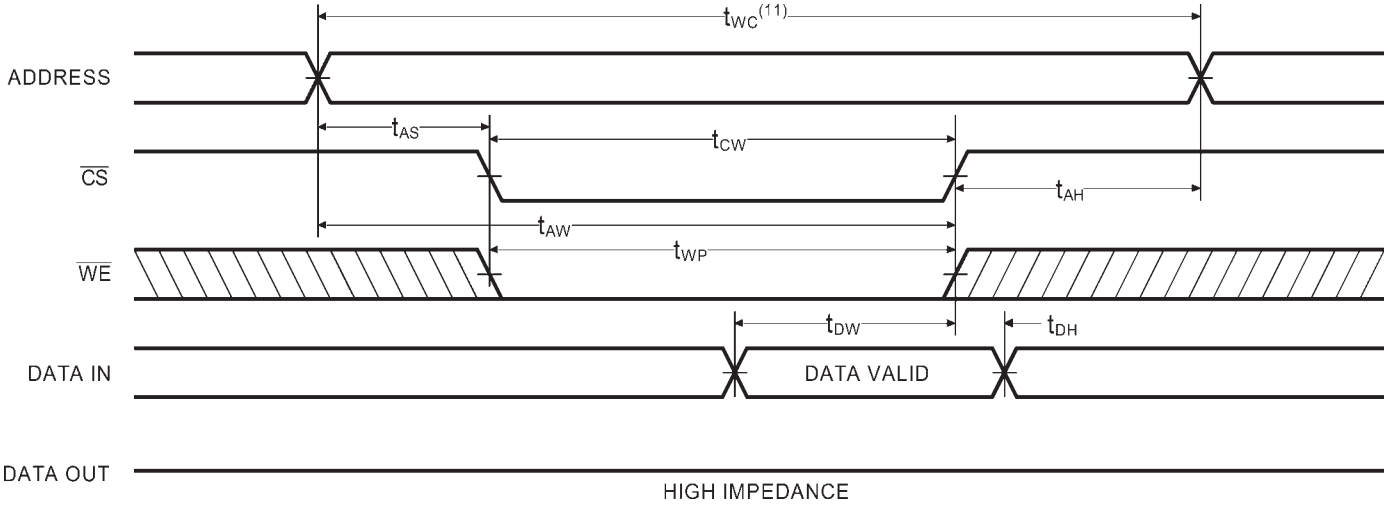
(V_{CC} = 5V ± 10%, All Temperature Ranges)(2)

Sym.	Parameter	-35		Unit
		Min	Max	
t_{WC}	Write Cycle Time	35		ns
t_{CW}	Chip Enable Time to End of Write	15		ns
t_{AW}	Address Valid to End of Write	15		ns
t_{AS}	Address Set-up Time	0		ns
t_{WP}	Write Pulse Width	15		ns
t_{AH}	Address Hold Time from End of Write	2		ns
t_{DW}	Data Valid to End of Write	15		ns
t_{DH}	Data Hold Time	2		ns
t_{WZ}	Write Enable to Output in High Z		15	ns
t_{OW}	Output Active from End of Write	0		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(9)



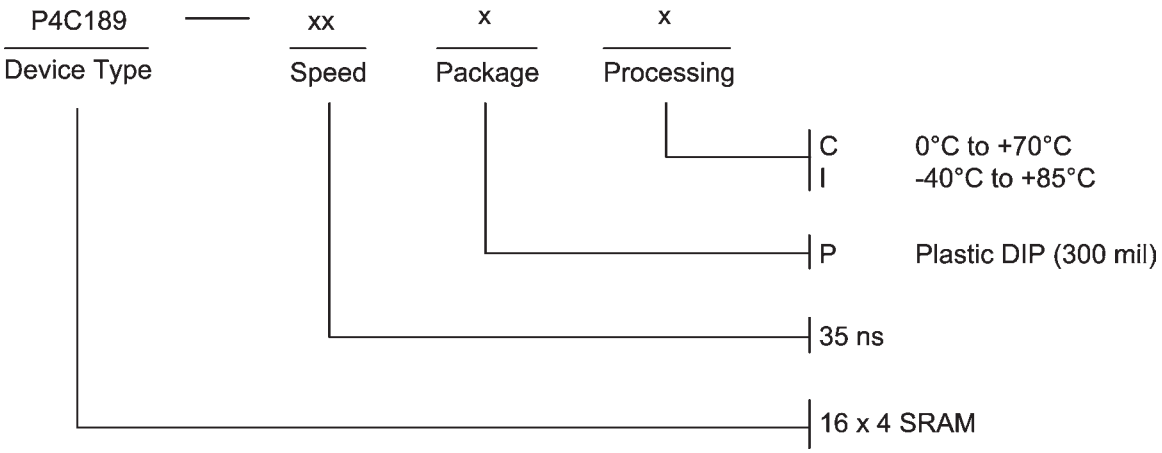
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[9]



Notes:

9. $\overline{CS}$ and $\overline{WE}$ must be LOW for WRITE cycle.
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
11. Write Cycle Time is measured from the last valid address to the first transition address.

ORDERING INFORMATION



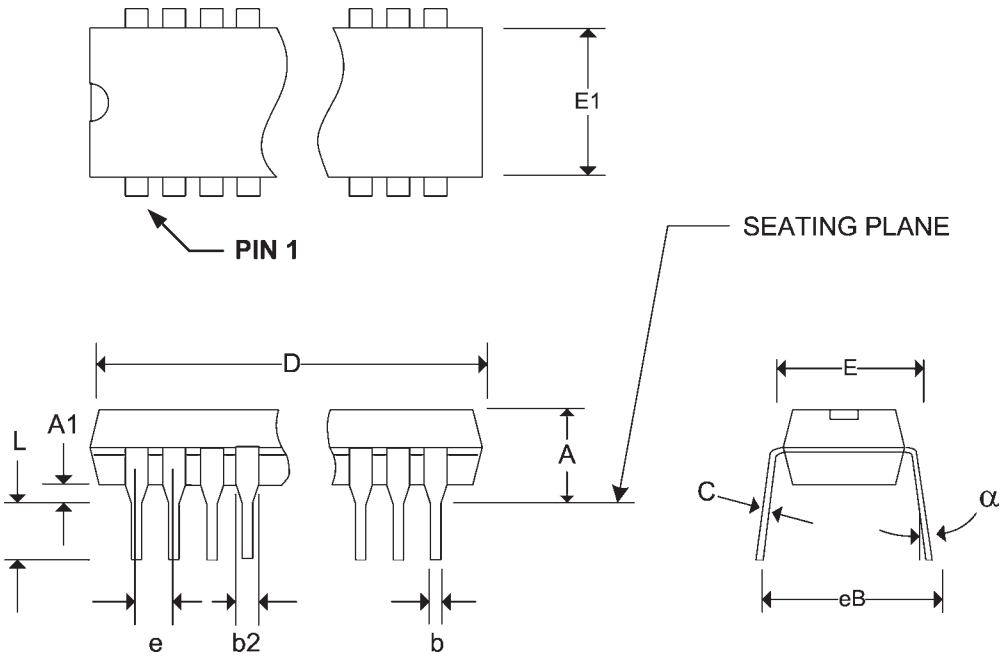
SELECTION GUIDE

The P4C189 is available in the following temperature range, speed, and package options.

Temperature Range	Package	Speed (ns)
		35
Commercial Temperature	Plastic DIP	-35PC
Industrial Temperature	Plastic DIP	-35PI

Pkg #	P7	
# Pins	16 (300 mil)	
Symbol	**Min**	**Max**
A	0.145	0.200
A1	0.020	-
b	0.014	0.023
b2	0.040	0.060
C	0.008	0.016
D	0.740	0.780
E1	0.240	0.260
E	0.300	0.320
e	0.100 BSC	
eB	0.310	0.365
L	0.125	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE



REVISIONS

DOCUMENT NUMBER:	SRAM100
DOCUMENT TITLE:	P4C189 HIGH SPEED 16 x 4 Static CMOS RAM with inverting outputs

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
OR	Oct-05	JDB	New Data Sheet