PYRAMID
SEMICONDUCTOR CORPORATION

1MB/4MB 5V Flash Product Flyer

FEATURES

- **Access Times of 55/70/90/120/150ns**
- **Single 5V±10% Power Supply**
- **Flexible Sector Architecture**
- **Low Power Consumption**
  - 20 mA Read current
  - 30 mA Program/Erase current
  - 1 µA Typical standby current
- **$\overline{\text{DATA}}$ Polling and Toggle Bits**

- **Erase Suspend/Resume**
  - Supports reading data from sectors not being erased.
- **Compatible with JEDEC standards**
  - Pinout/SW compatible with single-power supply Flash.
- **Sector Erase/Program Cycles 100K**
- **Data Retention: 20 Years @ 125°C**

DESCRIPTION

The PY29F010/040 is a family of 5 Volt 128K/512K x 8 Flash with a flexible sector architecture, supporting sector erasing and HW sector protections. With Access times of 55 to 150ns, and low power operation and designed to be programmed/erased in-system from a single 5.0V supply. The PY29F0x0 family is fully compatible with the JEDEC single power supply Flash standard.
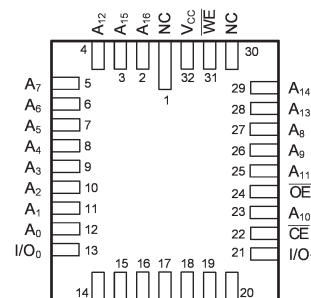
FUNCTIONAL BLOCK DIAGRAM
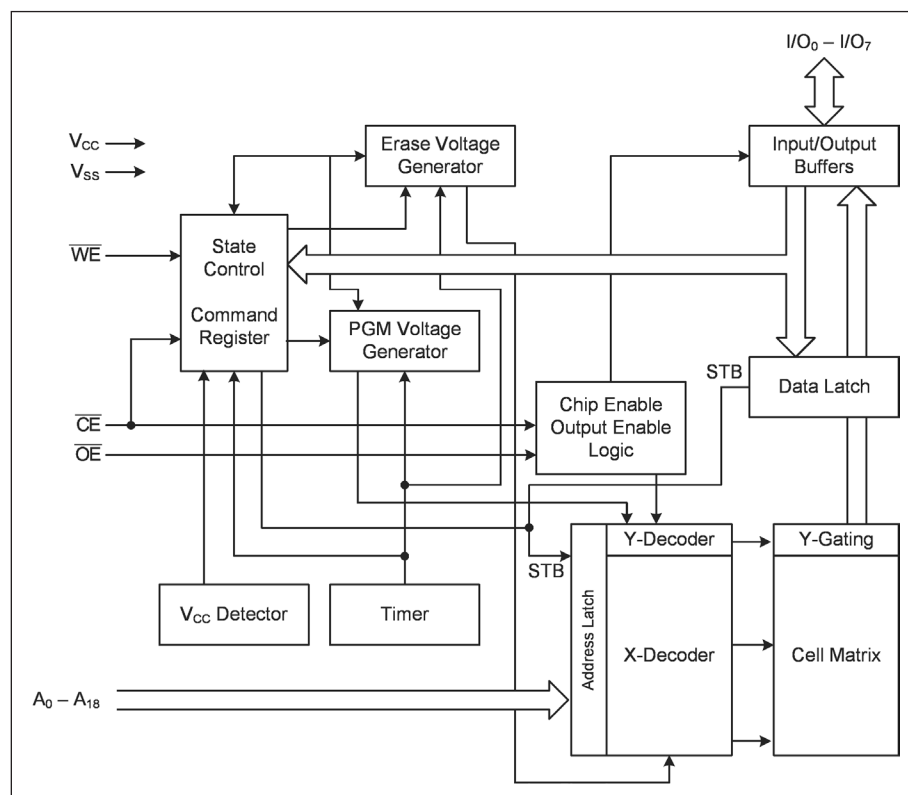
PIN CONFIGURATIONS
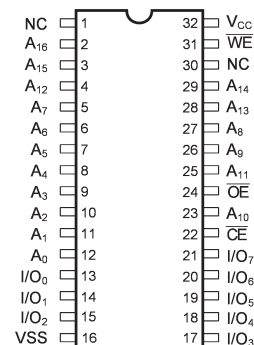
DIP (C10)

LCC (L6)

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OPERATION

The PY29F0x0 family is a 5.0 volt-only Flash memory organized as 131,072/524,288 bytes of 8 bits each. The 1MB has four 32K × 8 sectors, the 4MB device has eight 64K x 8 sectors for flexible sector erase capability. The 8 bits of data appear on I/O_0 - I/O_7 while the addresses are input on A_0 to A_{16}, for the 1MB, and A_0 to A_{18} for the 4MB. The PY29F0x0 Flash are offered in 32-pin ceramic LCC, Flatpack, and DIP packages. These devices are designed to be programmed in-system with only the standard system 5.0 volt V_{CC} supply.

The PY29F0x0 can also be programmed in standard EPROM programmers. The PY29F0x0 has the first toggle bit, I/O_6, which indicates whether an Embedded Program or Erase is in progress, or it is in the Erase Suspend. Besides the I/O_6 toggle bit, the PY29F0x0 have a second toggle bit, I/O_2, to indicate whether the addressed sector is being selected for erase.

The PY29F0x0 also offers the ability to program in the Erase Suspend mode. The standard PY29F0x0 offers access times of 55ns to 150ns allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The device requires only a single 5.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The PY29F0x0 are entirely software command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices. Device programming occurs by writing the proper program command sequence. This initiates the Embedded Program algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper program margin.

Device erasure occurs by executing the proper erase command sequence. This initiates the Embedded Erase algorithm - an internal algorithm that automatically pre-programs the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper erase margin.

The host system can detect whether a program or erase operation is complete by reading the I/O_7 (Data Polling) and I/O_6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The PY29F0x0 are fully erased (Set to "1") when shipped from the factory.

The hardware sector protection feature disables operations for both program and erase in any combination of the sectors of memory. This can be achieved via programming equipment.

The Erase Suspend feature enables the user to put erase on hold for any period of time to read data from, or program data to, any other sector that is not selected for erasure. True background erase can thus be achieved. Power consumption is greatly reduced when the device is placed in the standby mode.